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A Differential Measurement Probe with High Common Mode Rejection

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A Differential Measurement Probe with High Common Mode Rejection

Master's Thesis in Electrical Engineering

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Abstract

Measuring signals with high frequency common mode components are typically prone to measurement errors due to low common mode rejection at high frequencies. The purpose of this master thesis is to design a measurement probe that presents sufficient common mode rejection to measure current on high voltage motor drives directly at the switching stage, before filtering.

Outlined in this work is the design process, on a block diagram and simulation level, culminating in the construction of a prototype. The measurement probe consists of a sensor head and a receiver that are fiber optically isolated from each other. It has a signal chain that splits the signal into a high and a low frequency path. The high frequency path is frequency modulated and the low frequency path is digital. In the receiver, these two paths are joined before being output as an analog signal.

A signal chain is simulated that shows a DC-100 MHz response with an amplitude accuracy of 2.9 %, dynamic range of 53 dB, dropping to 38 dB at the end of the passband and, a spurious free dynamic range greater than 40 dB. Furthermore, a prototype is constructed but has not been debugged to a degree that permits meaningful measurement results.

Keywords: *Common mode rejection, Fiber-optic measurement probe, Current Sensing, High voltage measurements, Optical isolation*

Table of Contents

List of Variables

If the desired variable is not listed in this table, it is defined in the surrounding text where it is found.

Variable	**Description**
R_{DR}	Desired Dynamic Range.
R_{SFDR}	Desired Spurious Free Dynamic Range.
V_m	Modulating voltage in RMS.
$V_m(t)$	Modulating voltage, time dependent.
$V_m(s)$	Laplace transform of $V_m(t)$.
$\widehat{V_m}$	Modulating voltage, amplitude of sinusoid.
ω_0	FM signal center frequency in [rad/s].
f_m	Modulating frequency.
m	Modulation index.
C	SNR of the FM signal at demodulator input.
S	SNR of the demodulated signal due to the FM signal.
K_{VCO}	Voltage to frequency (Hz) gain of the VCO.
K_{PD}	Phase detector. Phase difference to voltage output.
P_{IF}	Phase detector. IF port power with 50 Ω load.
P_{RF}	Phase detector. RF port power with 50 Ω source.
P_{LO}	Phase detector. LO port power with 50 Ω source.
V_{IF}	Phase detector. Voltage at IF port with 50 Ω load.
G_{PD}	Phase detector. Conversion gain between RF- and IF port.
F_{PD}	Phase detector. Noise figure.
N_{IF}	Noise at phase detector IF port due to the phase detector.
N_{RF}	Noise at phase detector RF port.
$IP3_{IN}$	Phase detector. 3^{rd} order intermodulation product figure of merit.
R	Terminating impedance. Is always 50 Ω.
$A_{V,IF}$	Loop filter voltage gain. Defined from phase detector output to VCO input.
R_σ	Amplitude accuracy of the closed loop PLL. Only defined for fixed gain loop filters.
S_R	Amplifier slewrate.

$G_{VCO}(s)$	VCO input impedance.
$G_d(s)$	Delay element in PLL loop.
t_d	Propagation delay around the closed PLL loop.
L_p	Path length around the closed PLL loop.
P_{PHD}	Photodetector output power into 50 Ω.
N_{PHD}	Photodetector output noise into 50 Ω.
R_{IN}	Relative Intensity Noise of the laser. Equivalent to SNR at the photo detector output, if the detector is ideal.
S_{PHD}	SNR at photodetector output. Is shown to be equivalent to R_{IN}.

Chapter 1

Introduction

1.1 Background

Measuring differential signals with high frequency common mode components are prone to measurement errors due to low common mode rejection at high frequencies. For sufficiently high common mode frequencies, regular measurements, through an isolation transformer, is likely to offer inadequate common mode rejection. Especially so if the signal levels are also small and in the same frequency range as the common mode induced noise. This necessitates custom measurements systems with unconventional electrical isolation.

1.2 Purpose

The purpose of this master thesis is to design a measurement probe that presents sufficient common mode rejection to measure current on high voltage motor drives directly at the switching stage, before filtering. It is assumed that such a measurement scenario represents a common mode pulse voltage of 10 kV/µs, 500 $V_{pk\text{-}pk}$ and that the maximum signal voltage is 20 mV RMS. Furthermore, the signal frequency content is assumed limited to 100 MHz. The probe should be designed as a general purpose measurement tool, but the aforementioned scenario is used as reference.

1.3 Report Disposition

The report is organized as follows

- Section 2. “Theory” describes the measurement problem as well as the FM synthesis. It further describes a phase locked loop type FM demodulator and expressions for design parameters, from requirements such as spurious free dynamic range (SFDR) and dynamic range (DR), are derived. Additionally, a simulation model is derived.

- Section 3. “Implementation“ presents the proposed system and utilizes the derived expressions as the basis for choosing appropriate, real, components. Simulation parameters are obtained in a similar fashion.
- Section 4. “The Prototype” presents the designed protype and the philosophy behind its design.
- Section 5. “Results and Discussion” presents the simulation results and the models that are used. The status of the prototype is also elaborated upon.

Chapter 2
Theory

This chapter describes the measurement problem as well as the FM synthesis. It further describes a phase locked loop type FM demodulator and expressions for design parameters from requirements such as spurious free dynamic range (SFDR) and dynamic range (DR) are derived. A complete simulation model is also derived in order to model the signal chain.

2.1 Definition of Figure of Merits

To avoid ambiguous definition of figure of merits, the following definitions are used. The Dynamic Range (DR) is defined as

$$R_{DR} = \frac{V}{N_V} \tag{1}$$

Where V is the signal voltage amplitude in RMS and N_V is the RMS voltage noise integrated over the system bandwidth. The signal is a single sinusoid.

The Spurious Free Dynamic Range (SFDR) is defined as

$$R_{SFDR} = \frac{V}{D} \tag{2}$$

Where V is the voltage amplitude of the signal (single sinusoid) and D is the voltage amplitude of the largest spurious product. The signal can either be a single sinusoid or two signals of equal amplitude, depending on whether harmonics or intermodulation products are analyzed. If two signals are used, V is their individual amplitude.

The Signal to Noise ratio (SNR, S), and Carrier to Noise ratio (CNR, C) is defined as

$$C = S = \frac{P}{N} \tag{3}$$

Where P is the signal power in RMS and N is the noise power, in RMS, integrated over the system bandwidth.

2.2 Description of Measurement Problem

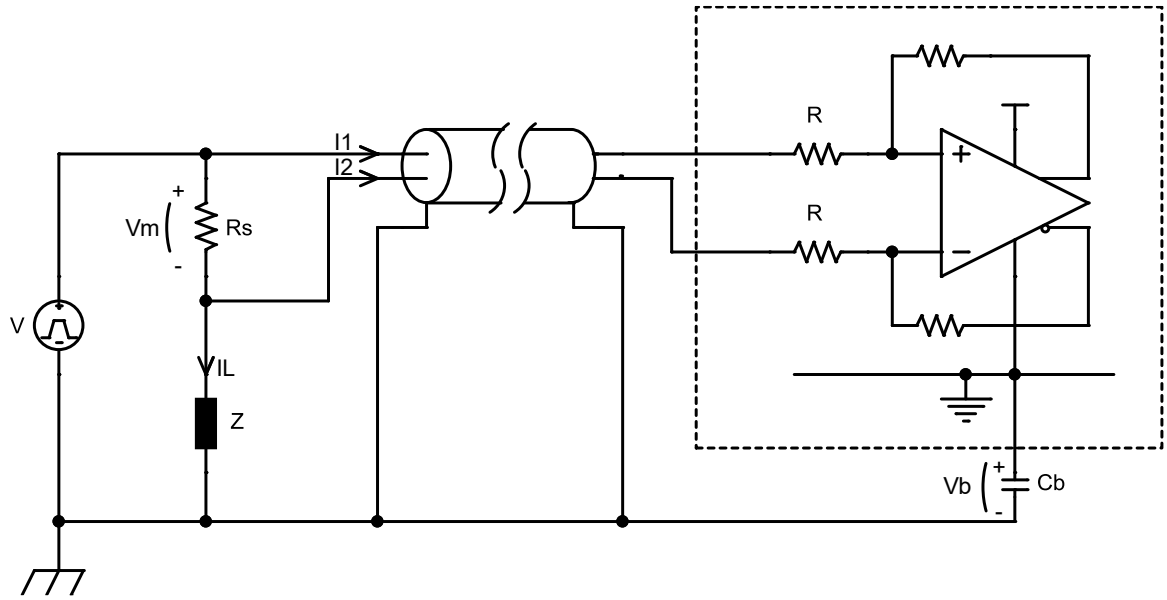

Figure 1 - An isolated amplifier measuring the voltage over a current shunt.

Consider the measurement setup shown in Figure 1. The intent is to measure the differential voltage over a current shunt, V_m, produced by applying a rectangular waveform, V, over a low impedance load, Z. This corresponds to a simplified representation of a switched motor drive. The voltage over the load is typically referred to as the common mode (CM) voltage. The common mode voltage is divided between the input resistors, R, and the isolation transformer. In Figure 1, the isolation transformer is represented by its interwinding capacitance, C_b, to reflect that it does not offer perfect isolation. To simplify the analysis, it is assumed that the secondary side of the transformer has its negative reference tied directly to protective earth. The same is assumed to be true for the measurement object. It is further assumed that protective earth represents an ideal reference plane such that the impedance between the two system's references is zero.

What is typically referred to as the CM voltage is not the CM voltage the amplifiers senses. If the input resistors are all equal, the amplifier common mode voltage is

$$\begin{aligned} V_{CM}(s) = \frac{I_1R + I_2R}{2} &= \frac{sC_bRV(RR_s + 2RZ + R_sZ)}{2(2RR_s + 2RZ + R_sZ + C_bR^2R_ss + C_bR^2Zs + C_bRR_sZs)} \\ &\approx \frac{s2ZC_bR^2V}{2\left(2RZ + sC_bR(RR_s + RZ + R_sZ)\right)} \approx \frac{sC_bRV}{2 + sC_b(R + R_s)} \\ &= V\frac{s\frac{C_bR}{2}}{1 + \frac{sC_bR}{2}} \approx sV\frac{C_bR}{2} \\ &\Rightarrow V_{CM}(t) \approx \frac{\Delta V}{\Delta t}\frac{C_bR}{2} \end{aligned} \quad (4)$$

Where the approximation is valid given $2R \gg R_S$, $2|Z| \gg R_S$, $\omega \gg 2/(C_bR)$, V is considered a step function and, the expression is evaluated only during the transition from high to low. $\Delta V/\Delta t$ is then the voltage derivative during the transition. The approximation shows that during the step transition, the entire voltage is applied over the isolation capacitance and produces a current which is drawn through the two input resistors. For a rectangular voltage, V, it means that the amplifier output will have small rectangular steps added on top of the desired signal. These steps have a time base equal the time it takes V to transit from low to high and occurs at each transition with alternating amplitude.

The amplifier's undesired output voltage, due to the CM voltage, is obtained from the CMRR figure of merit ($CMRR = A_{DM}/A_{CM}$) of the amplifier and its resistor network. It must be small enough not to impact the desired dynamic range. If the isolation barrier current through the shunt is much less than the current through the load, V_m is the desired signal. The following inequality must then hold,

$$\frac{A_{DM}}{C_{MRR}} V_{CM} < \frac{V_m A_{DM}}{R_{DR}} \tag{5}$$

Where C_{MRR} is the CMRR of the amplifier and its resistor network, R_{DR} is the desired dynamic range and, A_{DM} is the amplifier differential voltage gain. To show how stringent this requirement is, insert the approximation of Equation 4 into Equation 5.

$$\frac{1}{C_{MRR}} \frac{\Delta V}{\Delta t} \frac{RC_b}{2} < \frac{V_m}{R_{DR}} \Rightarrow C_b < \frac{2V_m C_{MRR}}{RR_{DR} \frac{\Delta V}{\Delta t}} = \frac{2 \cdot 20[\text{mV}] \cdot 1000}{50[\Omega] \cdot 1000 \cdot 10[\text{kV}] \cdot 10^6 \left[\frac{1}{\text{s}}\right]} = 80 \text{ fF} \tag{6}$$

Where arbitrary, but representative for the application at hand, values are used. Considering that a typical power transformer has a parasitic capacitance on the order of 10 pF, it is obvious that a simple isolation transformer is insufficient when dealing with small high frequency inputs signals as well as high common mode voltage derivatives. If the signal only has low frequency content, the requirement is much more relaxed as it may be low pass filtered to remove the high frequency common mode noise. In this thesis, the signal bandwidth is assumed to also include the common mode frequencies, making low pass filtering impossible.

It should also be noted that the CMRR will ultimately be limited by tolerances in the passive components and the cable between measurement point and amplifier. With resistors matched within 0.1 %, the CMRR is 66 dB [1], assuming not limited by the amplifier, cables or capacitors. Amplifiers with such excellent CMRR do exist, ADA4927

from Analog Devices has a CMRR 43 dB at 1 GHz and will thus not limit the CMRR, as the resistors matching specification can hardly be assumed valid at higher frequencies.

While the model is only meant to illustrate the measurement problem itself, factors such as line inductance between the measurement system and the system being measured, causes resonance where the isolation barrier impedance is close to zero. Modelling, and predicting, such behavior is not meaningful as it will depend on a given measurement setup. The bottom line, however, is that the isolation impedance should be maximized, and/or the voltage (derivative) over it minimized, to maximize the dynamic range of the measurement.

2.3 Frequency Modulation and Demodulation

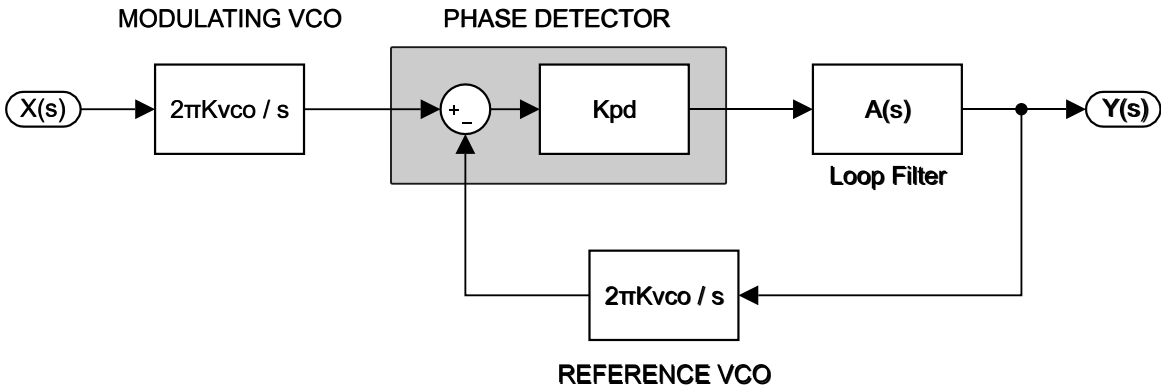

Figure 2 – Block representation of frequency modulation synthesis and demodulation by a phase locked loop.

Figure 2 shows the frequency modulation (FM) transmission chain which is analyzed in this section. The baseband modulating signal is passed to a voltage-controlled oscillator (VCO), which converts it to an FM signal. The modulated FM signal is then passed through a transmission chain consisting of amplifiers and the transmission medium itself. To demodulate the signal, its phase is compared to that of a reference VCO by a phase detector. The input to the reference VCO is connected to the output of the phase detector through a filter, forcing it to track the incoming FM signal. Thus, the input to the reference VCO corresponds to the original baseband signal. The demodulator is referred to as a phase-locked loop (PLL).

While different types of demodulators exist, a PLL-type demodulator is assumed to provide by far the highest linearity. This is mainly due to the fact that if the VCO is modulated by a signal with high amplitude, its voltage to frequency gain is not constant. Using a high amplitude is imperative if both high dynamic range and, a large frequency range, is desired. If the demodulator cannot implement the exact inverse frequency to voltage relationship, there will be distortion. In this case, a PLL offers the ideal solution as the same type of VCO can be used in both modulator and demodulator and thus negate any non-linearity due to the VCO.

Frequency modulation has several appealing qualities which makes it suitable for the application at hand. The most important property is its ability to trade bandwidth for signal to noise ratio. It is also insensitive to changes in FM signal power, since amplitude limiters can be used to remove any variation.

It is, however, sensitive to non-flat transfer characteristics. If the transmission chain between modulating VCO and PLL, or between reference VCO and phase detector, does not have flat amplitude and phase characteristic, the demodulated signal will exhibit both amplitude ripple over frequency as well as distortion. Both issues can be diminished if care is taken to make both paths behave similarly. This may be understood by noting that the reason both distortion and amplitude ripple occurs, is because the reference VCO is attempting to track the modulating VCO but has no ability to do so perfectly because the different paths changes the signal. Make both paths equal and the only possible loss is in SNR, because part of the information is lost if the paths are not flat in frequency. To further strengthen the argument, the analysis presented in [2] shows distortion approaching zero if both paths are equal, both VCOs are of the same type and a linear phase detector is used. In practice, non-linearity in the phase detector is assumed to be the limiting factor. As such, the analysis given in the following section considers the transmission medium, and the related amplifiers, to have a flat phase and frequency characteristic.

This chapter gives a description of the FM synthesis as well as a demodulation scheme. Emphasis is, however, put on the derivation of expressions for requirements imposed on each building block. Furthermore, a simulation model suitable for SPICE simulations is derived.

2.3.1 The Frequency Modulated Signal

A frequency modulated signal is obtained by applying a baseband signal to the input of a voltage-controlled oscillator. The VCO has an output frequency dependent on the voltage applied at its input.

$$\begin{aligned} \omega_{VCO} &= \omega_0 + 2\pi K_{VCO} V_m(t) \\ \Rightarrow \phi_{VCO} &= \int_0^t [\omega_0 + 2\pi K_{VCO} V_m(t)]dt = \omega_0 t + 2\pi K_{VCO} \int_0^t V_m(t)dt \end{aligned} \tag{7}$$

Where K_{VCO} is the VCO gain, ω_0 is the FM center frequency (dependent on the bias voltage) and, $V_m(t)$ is the baseband signal voltage applied to the VCO. The VCO output signal can then be described by

$$V_o(t) = V\sin(\phi_{VCO}) = V\sin\left(\omega_0 t + 2\pi K_{VCO}\int_0^t V_m(t)dt\right) \tag{8}$$

Where V is the (fixed) amplitude of the FM signal set by the VCO. For larger deviations from the bias voltage, the first order approximation of the VCO gain as constant does not hold and the output frequency will be dependent on higher order terms of the applied

voltage as well. The theory presented here assumes the validity of the first order approximation and it is simply noted that expressions becomes increasingly invalid as amplitude deviations increase.

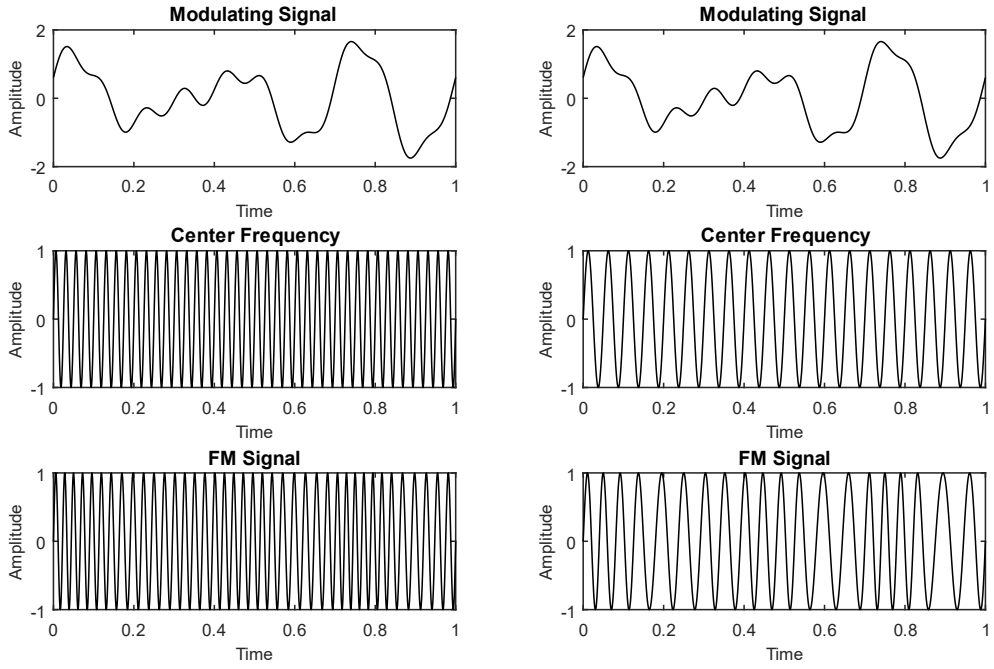

Figure 3 – Time domain representations of two FM signals with the same baseband signal but different center frequencies.

Figure 3 shows two arbitrary FM signals. Their baseband version is the same, but the center frequency is different. The lowest center frequency corresponds to twice the highest frequency in the baseband signal. It illustrates what is evident in Equation 8, that FM signals have constant power, independent of modulating signal. It further shows, at least circumstantially, that the phase variations do not cause the FM signal to lose its sinusoidal shape. By analyzing Equation 8 it is seen that

$$f_0 t \gg K_{VCO} \int_0^t V_m(t)dt \Rightarrow V_o(t) \approx V \sin(\omega_0 t) \tag{9}$$

Which means that if the center frequency is sufficiently large, the FM signal will behave sinusoidally. This result is of interest when analyzing the phase detector.

Since superpositions cannot be used when analyzing FM signals, evident from Equation 8 because of the sine term, a description in the frequency domain must be evaluated for each type of modulating signal. A sinusoid, for an example is described by [3].

$$V_o(t) = V \sum_{n=-\infty}^{\infty} J_n(m)\sin(2\pi t(f_0 + nf_m)) \tag{10}$$

Where J_n is a Bessel function of the first kind of the n:th order, $m = K_{VCO}\hat{V}_m/f_m$ is the modulation index, f_m the baseband frequency, f_0 is the center frequency of the modulated signal and, $\hat{V}_m$ is the amplitude of the input signal.

If the applied baseband signal is rectangular [3],

$$V_o(t) = V \sum_{n=-\infty}^{\infty} \frac{m}{\pi(m-n)(mD-nD+n)} \sin\big(\pi D(m-n)\big) \sin(2\pi t(f_0 + nf_m)) \tag{11}$$

Where $m = K_{VCO}\hat{V}_m/f_m$ is the modulation index, D the duty cycle of the rectangular input, f_m its fundamental frequency, f_0 is the center frequency of the modulated signal and, $\hat{V}_m$ is the peak to peak amplitude of the input signal. The center frequency is given by the sum of the DC level of the rectangular input and the bias voltage applied at the VCO input and, multiplied by the VCO gain, K_{VCO}. V is the amplitude of the wave, defined by V^2 being equal to the sum of each term squared. The signal thus has constant energy as expected.

The expression shows discretely positioned frequency components spaced at even integers of the modulating frequency around the center frequency. It also shows how the amplitude of these components are dependent only on the modulating index for a given rectangular input. Even though the spectrum extends to infinity, most of the energy is contained close to the center frequency because the amplitude falls of as $1/n^2$ as $n \to \pm\infty$.

Another point to note is that for $n = 0$, the amplitude is a sinc function, $E\text{sinc}(\pi Dm)$. Thus, as the modulation index approaches zero, the signal energy is constrained to the center frequency. Since the center frequency is only dependent on the bias level of the signal, it does not contain any information (if one assumes that the signal DC level is not part of the signal) as is seen by noting that f_m vanishes for $n = 0$. Consequently, a lower limit is imposed on the modulation index. An estimation of this limit can be made from the demodulated SNR, to the received SNR at the demodulator input, relationship, valid for large CNR [4].

$$S = 3m^2(m+1)C \approx 3m^2C, \quad m \ll 1 \tag{12}$$

Where C is the signal to noise ratio input to the PLL and S is the signal to noise ratio at the PLL output. For a sinusoidal input, $m = K_{VCO}\hat{V}_m/f_m$ where the hat notation implies the amplitude of the sinusoid. Replacing m in Equation 12, and rearranging in terms of frequency, gives

$$m = \frac{K_{vco}\hat{V}_m}{f_m} \approx \sqrt{\frac{S}{3C}} \Leftrightarrow f_m \approx K_{vco}\hat{V}_m\sqrt{\frac{3C}{S}} \tag{13}$$

Noting that V_m is greatest, by definition, at the maximum SNR, which must be greater than the square of the desired dynamic range, i.e. $S > R_{DR}^2$, yields an upper frequency limit according to

$$f_m < K_{vco} \cdot \max\{\hat{V}_m\}\frac{\sqrt{3C}}{R_{DR}} \tag{14}$$

To maximize this limit, it is necessary to maximize both the received FM signal strength and the peak modulating voltage.

An estimate of the required bandwidth may be obtained from Carson's Rule, $B \approx 2(m + 1)f_m$. It is defined for a sinusoidal modulating voltage but is here assumed to be approximately accurate for all signals.

$$B \approx 2(m+1)f_m = 2\left(K_{vco}\hat{V}_m + f_m\right) \leq 2(K_{vco} \cdot \max\{\hat{V}_m\} + \max\{f_m\}) \tag{15}$$

To summarize, Equation 14 describes the maximum modulating frequency based on a desired dynamic range and Equation 15 in turn gives the required bandwidth.

2.3.2 Modulation and Demodulation

The phase-locked loop operates by comparing the phase of an input signal to that of a reference. The reference signal is produced by a VCO with its input connected to the output of the phase detector through a filter. Since the reference VCO is connected in a closed loop with the phase detector, and thus forced to track the input signal, its input is equal to the original baseband signal. Following is a description of each element in the PLL. Emphasis is put on the derivation of requirements imposed on each building block as well as obtaining a model suitable for SPICE simulations.

2.3.2.1 The Control Loop

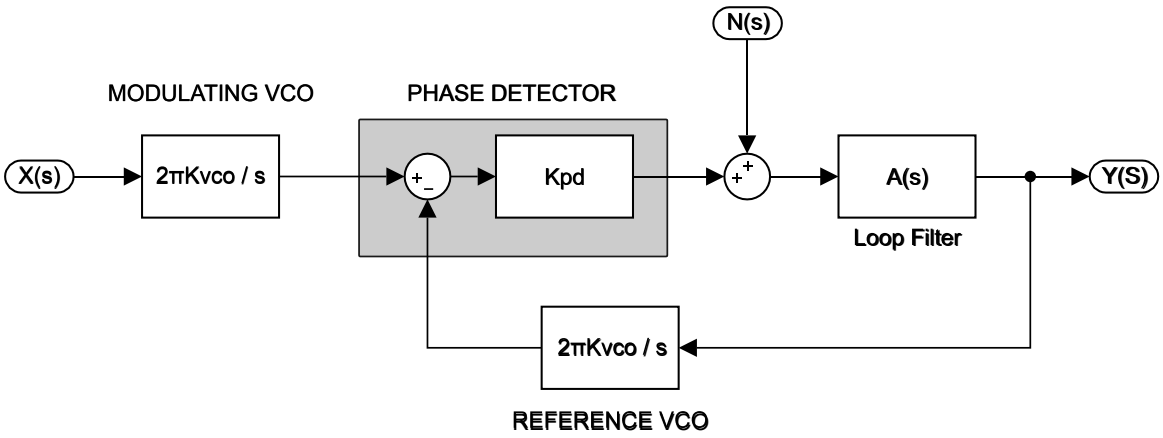

Figure 4 – The control loop simplified.

The control loop given in Figure 4 has the following transfer function between output and input.

$$\frac{Y(s)}{X(s)} = \frac{\frac{2\pi K_{VCO}}{s} K_{PD} A(s)}{1 + \frac{2\pi K_{VCO}}{s} K_{PD} A(s)} = \frac{2\pi K_{VCO} K_{PD} A(s)}{s + 2\pi K_{VCO} K_{PD} A(s)} \tag{16}$$

It is of interest to derive the type of loop filter, A(s), which gives the optimal response. This may be done by considering the output error.

$$\begin{aligned} E(s) = X(s) - Y(s) = X(s) - X(s) \cdot \frac{Y(s)}{X(s)} = X(s)\left[1 - \frac{2\pi K_{VCO} K_{PD} A(s)}{s + 2\pi K_{VCO} K_{PD} A(s)}\right] \\ = X(s) \frac{s}{s + 2\pi K_{VCO} K_{PD} A(s)} \end{aligned} \tag{17}$$

The steady state error can be evaluated by the final value theorem. Let the input be a ramp, $X(s) = 1/s^2$, and the loop gain be on the form $K_L/(1+s/\omega_1)^2$, describing two amplifiers with no feedback resistor. K_L is the amplifier open loop gain and ω_1 is the amplifier open loop gain cut-off frequency. The steady state error is then

$$\begin{aligned} \lim_{t\to\infty} e(t) = \lim_{s\to 0} sE(s) = \lim_{s\to 0} sX(s) \frac{s}{s + 2\pi K_{VCO} K_{PD} A(s)} = \lim_{s\to 0} \frac{s}{s^2} \frac{s}{s + \frac{2\pi K_{VCO} K_{PD} K_L}{\left(1 + \frac{s}{w_1}\right)^2}} \\ = \lim_{s\to 0} \frac{\left(1 + \frac{s}{w_1}\right)^2}{s\left(1 + \frac{s}{w_1}\right)^2 + 2\pi K_{VCO} K_{PD} K_L} = \frac{1}{2\pi K_{VCO} K_{PD} K_L} \approx 0 \end{aligned} \tag{18}$$

That is, for the system to transmit a ramp function with no error, the loop filter needs to have at least one pole at s = 0, implementing an integrator. Since real amplifiers have limited gain, and cannot truly implement integrators, there will always be a steady-state error for a ramp input. This error, however, is negligible as $K_{VCO} > 10^6$. There is also no downside to having the amplifiers in open loop, as is seen by analyzing the noise gain.

The noise associated with the phase detector, stemming mainly from noise picked up in the transmission channel between modulating VCO and the PLL input, is expected to be the largest. The noise gain from the phase detector output to the PLL output is

$$\frac{Y(s)}{N(s)} = \frac{A(s)}{1 - K_{PD}\frac{2\pi K_{VCO}}{s}A(s)} = \frac{sA(s)}{s - K_{PD}2\pi K_{VCO}A(s)} \tag{19}$$

A plot of Equation 19 is given in Figure 5 for two different loop filters. “Integrating”, $A(s) = K_L/(1 + s/\omega_1)^2$, corresponding to two amplifiers with no feedback coupling, and “Fixed Gain”, $A(s) = 10^3$.

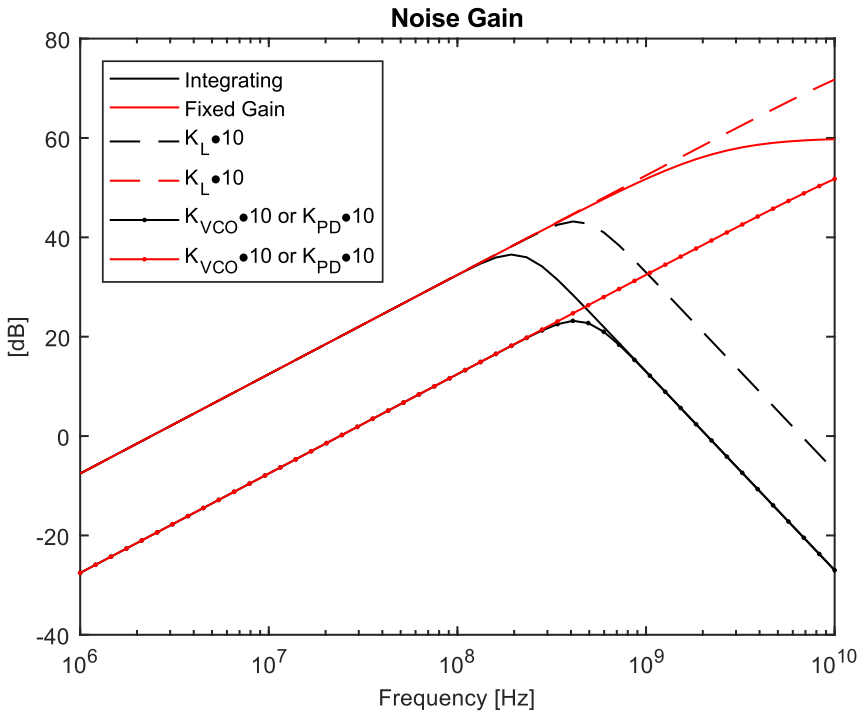

Figure 5 – Noise gain as predicted by Equation 19. The solid lines correspond to values representative for the final design. The dotted and dashed lines correspond to changes in one variable. Colors correspond to filter types.

It is seen that higher VCO or phase detector gain decreases the noise gain while higher loop gain increases it. Since the given loop filters do not account for additional low pass filtering within the loop, the effect of increasing the loop gain is likely to fall outside the passband and can thus be expected to only negligible increase the noise gain. Increasing

either VCO gain or phase detector gain is seen to substantially decrease the noise. It is, however, seen in Section 2.3.2.2 that an increase in phase detector gain increases spurs and as such, imposes an upper limit on the phase detector gain. Similarly, the VCO gain is fixed for a given VCO. While shifting the bias voltage of the VCO changes the gain, it is not practically possible. If large amplitude deviations are required, which it will be as this increases DR, the VCO gain remains more or less fixed because it is desirable to have the VCO operating over a relatively constant gain region. Furthermore, higher VCO gain means higher phase noise, as amplitude variation on its input gets converted into phase variation. The conclusion to be drawn is that the noise gain cannot be changed independently but is instead set by design requirements imposed by SFDR and DR.

2.3.2.2 The Phase Detector

The phase detector is a double balanced mixer. It is the device of choice as the linearity of digital phase detectors is poor at high frequencies. The linearity of the mixer, on the other hand, can be made high at the expense of lower input power. However, as is seen in Section 2.3.2.1, lower power means higher amplitude noise and thus might limit the dynamic range. Presented here is the fundamental principle behind the mixer as phase detector, followed by a description in the frequency domain and the requirements it imposes on surrounding circuitry.

Two input voltages, $v_1 = V_1\cos(\omega_o t + \phi_1(t))$ and $v_2 = V_2\cos(\omega_o t + \phi_2(t))$, applied to the RF and LO port of an ideal mixer produces the output

$$V_{IF}(t) = v_1(t)v_2(t) = \frac{V_1V_2}{2}\left[\cos(2\omega_o t + \phi_1(t) + \phi_2(t)) + \cos\left(\phi_1(t) - \phi_2(t)\right)\right] \qquad (20)$$

Where it can be shown that the same result is obtained if the inputs are sinusoidal. If the $2\omega_0$ term is removed by filtering, it is apparent the output has a sinusoidal relationship to the phase difference between the LO and RF port. The two cosine terms correspond to the two sidebands. The power in one of these can be obtained from the conversion gain listed in the mixer's datasheet. Conversion gain relates the power at the RF port to the power in one sideband at the IF port, for a given LO port power. The figure of merit is determined under the assumption that a single sinusoid is applied to the LO port and that all terminals are matched. Since an FM signal consists of several frequencies, it is not obvious at the onset that this relationship is applicable. However, if the center frequency is sufficiently high, the FM signal is piece wise sinusoidal as is circumstantially shown in Figure 3. As

such, assume that the conversion gain is valid for FM signals as well. Then, the phase detector output power is

$$P_{IF} = P_{RF}G_{PD} \tag{21}$$

Where G_{PD} is the conversion gain, P_{IF} is the IF port power in one sideband and P_{RF} is the RF port power. Rewriting power into peak voltage and multiplying it with the cosine scaling factor of Equation 20, the IF voltage is

$$V_{IF}(t) = \sqrt{2G_{PD}P_{RF}R}\cos(\phi_{RF}(t) - \phi_{LO}(t)) \tag{22}$$

Where R is the matching impedance, typically 50 Ω.

For an FM signal, the input at the RF and LO port may be rewritten as $v_1 = \cos(\omega_o t + 2\pi K_{VCO}\int x(t)dt)$ and $v_2 = \cos(\omega_o t + 2\pi K_{VCO}\int y(t)dt - \phi_2)$. Where x(t) and y(t) is the input signal to the VCO in the modulator and PLL respectively. Using Equation 22,

$$\begin{aligned} V_{IF}(t) &= \sqrt{2G_{PD}P_{RF}R}\cos\left(2\pi K_{VCO}\int x(t)dt - 2\pi K_{VCO}\int y(t)dt + \phi_2\right) \\ &\approx 2\pi K_{VCO}\sqrt{2G_{PD}P_{RF}R}\left[\int x(t)dt - \int y(t)dt\right] \end{aligned} \tag{23}$$

The last approximation is valid given $\phi_2 = \pi/2$ and a small enough phase variation such that $\cos(x + \pi/2) = \sin(x) \approx x$ holds. Taking the derivative yields,

$$\frac{dV_{IF}(t)}{dt} = 2\pi K_{VCO}\sqrt{2G_{PD}P_{RF}R}[x(t) - y(t)] \tag{24}$$

Assume that the PLL is locked and that the input to the PLL VCO is $y(t) = \hat{V}_m\sin(\omega_{mod}t)$. Let the loop gain be constant with frequency and as such be independent of time. Then, the output from the phase detector is y(t) divided by the loop gain. By taking the derivative,

$$\frac{dV_{IF}}{dt} = \frac{d}{dt}\frac{\hat{V}_m\sin(\omega_m t)}{A_{V,IF}} = \frac{\hat{V}_m\omega_m\cos(\omega_m t)}{A_{V,IF}} \tag{25}$$

and inserting into Equation 24 together with y(t),

$$\begin{aligned}&\frac{\hat{V}_m\omega_m\cos(\omega_m t)}{A_{V,IF}} = 2\pi K_{VCO}\sqrt{2G_{PD}P_{RF}R}\left[x(t) - \hat{V}_m\sin(\omega_m t)\right]\\ &\Leftrightarrow x(t) = \frac{\hat{V}_m f_m}{K_{VCO}A_{V,IF}\sqrt{2G_{PD}P_{RF}R}}\cos(\omega_m t) + \hat{V}_m\sin(\omega_m t)\end{aligned} \tag{26}$$

For the PLL to track correctly, x(t) must be equal y(t). It is seen that for the PLL to demodulate the signal contained within the incoming FM signal correctly, the amplitude of the cosine term must approach 0. A gain requirement may be derived from this in terms of accuracy. Express x(t) and y(t) in RMS and denote their ratio σ. Their ratio expresses how much the signal deviates from the expected, i.e. it represents the accuracy/amplitude ripple.

$$\begin{aligned}\sigma^2 &= \frac{\int_T x(t)^2 dt}{\int_T y(t)^2 dt}\\ &= \frac{\frac{\pi}{\omega_m}\left[\left(\frac{\hat{V}_m f_m}{K_{VCO}A_{V,IF}\sqrt{2G_{PD}P_{RF}R}}\right)^2 - 2\frac{\hat{V}_m f_m}{K_{VCO}A_{V,IF}\sqrt{2G_{PD}P_{RF}R}}\hat{V}_m + \hat{V}_m^2\right]}{\frac{\pi}{\omega_m}\hat{V}_m^2}\\ &= \left(\frac{f_m}{K_{VCO}A_{V,IF}\sqrt{2G_{PD}P_{RF}R}}\right)^2 - \frac{2f_m}{K_{VCO}A_{V,IF}\sqrt{2G_{PD}P_{RF}R}} + 1\end{aligned} \tag{27}$$

For the amplitude to be within a given accuracy, R_σ, the following inequality must hold

$$(1 - R_\sigma)^2 < \left(\frac{f_m}{K_{VCO}A_{V,IF}\sqrt{2G_{PD}P_{RF}R}}\right)^2 - \frac{2f_m}{K_{VCO}A_{V,IF}\sqrt{2G_{PD}P_{RF}R}} + 1 < (1 + R_\sigma)^2 \tag{28}$$

Set the accuracy equal to its limit and solve for gain,

$$\begin{aligned}A_{V,IF} &= \frac{\pm\sqrt{f_m^2(1 \pm R_\sigma)^2} - f_m}{K_{VCO}\sqrt{2G_{PD}P_{RF}R}[(1 \pm R_\sigma)^2 - 1]} \approx \frac{\pm\sqrt{f_m^2(1 \pm 2R_\sigma)} - f_m}{K_{VCO}\sqrt{2G_{PD}P_{RF}R}[\pm 2R_\sigma]}\\ &= \left\{\frac{-\sqrt{f_m^2(1 - 2R_\sigma)} - f_m}{K_{VCO}\sqrt{2G_{PD}P_{RF}R}[-2R_\sigma]}, \quad \frac{+\sqrt{f_m^2(1 + 2R_\sigma)} - f_m}{K_{VCO}\sqrt{2G_{PD}P_{RF}R}[+2R_\sigma]}\right\}\\ &= \left\{\pm\frac{\sqrt{f_m^2(1 - 2R_\sigma)} + f_m}{2R_\sigma K_{VCO}\sqrt{2G_{PD}P_{RF}R}}, \quad \frac{\sqrt{f_m^2(1 + 2R_\sigma)} - f_m}{2R_\sigma K_{VCO}\sqrt{2G_{PD}P_{RF}R}}\right\}\\ &\approx \left\{\frac{f_m}{R_\sigma K_{VCO}\sqrt{2G_{PD}P_{RF}R}}, \quad 0\right\}\end{aligned} \tag{29}$$

Where the last approximation is valid for all practical accuracies and the negative solutions are discarded. As the function bounded in Equation 28 converges to 1 as the gain

approaches infinity, the highest valued solution should be chosen. Rewriting in terms of a limit,

$$A_{V,IF} > \frac{f_m}{R_\sigma K_{VCO}\sqrt{2G_{PD}P_{RF}R}} \tag{30}$$

Equation 30 thus states the gain requirement to arrive at a given accuracy. A reasonable value for the accuracy is to set it equal the gain ripple of the entire signal chain, around 2-5 % (~0.2 to ~0.6 dB amplitude ripple). Note that the expression only yields an approximate value as the loop gain is assumed constant in the previous integration. Since this will not be the case in practice, even fixed gain amplifiers have phase shift, it gives no information about stability and if the loop gain and phase is not constant inside the PLL passband, the expression is not valid. It does, however, serve as a good starting point for determining the required gain.

As is assumed in Equation 23, when the loop is locked, the phase difference between the RF and LO port is close to $\pm\pi/2$ as any control loop strives to bring its error to zero. Furthermore, for phase differences equal to $n\pi$, $n \in Z$, the loop loses its lock. This can be understood by noting that at π and 0, the derivative of cosine in Equation 22 changes sign and as such represents a discontinuity. The effect is a lower limit for the IF amplifier gain when $\phi_{RF} - \phi_{LO} = \pm\pi$.

A stricter gain requirement can be obtained by considering the required spurious free dynamic range. Expanding the cosine term of Equation 22 into a 3rd order Maclaurin series around $-\pi/2$ yields

$$\cos(x) = x + \frac{\pi}{2} - \frac{\left(x + \frac{\pi}{2}\right)^3}{6} + O(x^5) \tag{31}$$

Then, let the input be sinusoidal around its operating point, $x = -\pi/2 + a\cos(x) + b\cos(y)$ i.e. let the PLL demodulate an FM signal containing two sinusoids with different amplitudes and frequency.

$$\begin{aligned}\cos\left(-\frac{\pi}{2}+a\cos(x)+b\cos(y)\right)&\\ &= a\cos(x)+b\cos(y)\\ &-\frac{1}{24}[3a^3\cos(x)+a^3\cos(3x)+\ 3a^2b\cos(2x-y)\\ &+\ 3a^2b\cos(2x+y)+6a^2b\cos(y)+\ 3ab^2\cos(x-2y)\\ &+\ 3ab^2\cos(x+2y)+6ab^2\cos(x)+3b^3\cos(y)+b^3\cos(3y)]\\ &+O(x^5)\\ &\approx a\cos(x)+b\cos(y)\\ &-\frac{1}{24}[(a^3\cos(3x)+3a^2b\cos(2x-y)+3a^2b\cos(2x+y)\\ &+3ab^2\cos(x-2y)+3ab^2\cos(x+2y))+b^3\cos(3y)]\end{aligned} \tag{32}$$

Where the approximation holds if a,b $\ll 1$ (i.e. small variation in phase difference) and the higher order terms are considered small. If $a = b = A \ll 1$, the largest spurs have amplitude $3A^3/24$. The spurious free dynamic range can be approximated by the ratio between the amplitude of the fundamental and the spur with highest value i.e.

$$R_{SFDR} = \frac{A}{\left(\frac{3A^3}{24}\right)} = \frac{24}{3A^2} \tag{33}$$

Which can be rewritten as an inequality for the largest signal amplitude at the IF port for a given SFDR.

$$A < \sqrt{\frac{24}{3R_{SFDR}}} \tag{34}$$

Let $\phi_{RF} - \phi_{LO} = -\pi/2 + A\cos(x) + A\cos(y)$, where $x = \omega_1 t$ and $y = \omega_2 t$ and insert into Equation 22.

$$\begin{aligned}V_{IF} \approx \sqrt{2G_{PD}P_{RF}R}\cdot A[\cos(\omega_1 t)+\cos(\omega_2 t)] &= \frac{\hat{V}_m}{A_{V,IF}}[\cos(\omega_1 t)+\cos(\omega_2 t)]\\ \Rightarrow A_{V,IF} &= \frac{\hat{V}_m}{A\sqrt{2G_{PD}P_{RF}R}}\end{aligned} \tag{35}$$

Where the last equality must hold for the loop to be locked. The assumption as made that the gain has no phase shift. By inserting Equation 34, the minimum IF gain to achieve a given SFDR is

$$A_{V,IF} > \frac{\max\{\hat{V}_m\}}{\sqrt{\frac{1}{R_{SFDR}}\cdot\frac{24}{3}}\sqrt{2G_{PD}P_{RF}R}} = \max\{\hat{V}_m\}\sqrt{\frac{3R_{SFDR}}{48RP_{RF}G_{PD}}} \tag{36}$$

Equation 36 thus represents a minimum loop filter gain, to achieve a given SFDR. Equation 36 may also be rearranged in terms of SFDR,

$$R_{SFDR} = \frac{48A_{V,IF}^2 G_{PD} P_{RF} R}{3\hat{V}_m^2} \tag{37}$$

Where it is seen that the SFDR is improved by the square of the loop gain. The expression is only strictly valid if the gain has no phase shift.

From the perspective of previous equations, the higher the RF port power, the better. However, in real mixers, increasing input power increases distortion. An upper limit of RF input power is set by the third order intermodulation products of the mixer. This has not yet been considered as the mixer has thus far been assumed ideal. The IM3 spectrum is given by [5]. If adopted to FM signals it may be rewritten as

$$\begin{aligned} f_{IM3} \in & \left\{ \begin{matrix} \left|\left(2(f_0 + nf_m) - (f_0 + mf_m)\right) - f_{LO}\right| , \\ \left|\left(2(f_0 + mf_m) - (f_0 + nf_m)\right) - f_{LO}\right| \end{matrix} \right\} \\ & = f_o - f_{LO} + f_m\{|2m - n|, |2n - m|\}, \qquad m, n \in Z, m \neq n \end{aligned} \tag{38}$$

Where f_{LO} is a single frequency component at the LO port. If the signal at the LO port is also an FM signal,

$$\begin{aligned} f_{IM3} \in & \left\{ \begin{matrix} \left|\left(2(f_0 + nf_m) - (f_0 + mf_m)\right) - (f_0 + lf_m)\right| , \\ \left|\left(2(f_0 + mf_m) - (f_0 + nf_m)\right) - (f_0 + lf_m)\right| \end{matrix} \right\} \\ & = f_{mod}\{|2n - m - l|, |2m - n - l|\}, \qquad m, n, l \in Z, m \neq n \end{aligned} \tag{39}$$

Where it is apparent that IM3 products is present within the baseband. It remains to ascertain their magnitude. Consider a theoretical FM signal which only has two spectral components centered around its center frequency and at equal distance, due to the symmetry of the FM signal. The power in each are half the total signal power. If the PLL is locked, the LO port will have the same signal. Then the output frequencies must be, with $n = -m = \pm 1$, $x \in Z\backslash\{0\}$ and $l \in \{-1, 1\}$, $f_{IM3} \in f_m\{|-3m - l|, |3m - l|\} = f_m\{|-3-1|, |-3+1|, |3-1|, |3+1|\} = f_m\{2, 4\}$. This is the same spectrum as obtained if LO is just a single frequency, but the power in each term is up to double. If one assumes that the phase difference between the LO and RF signals are such that the four components interact fully, the SFDR is degraded by 3 dB in relation to an LO consisting of a single frequency. The relation between IP3 product and RF port power given in [6] may be adopted to give the inequality

$$\begin{aligned} P_{RF}[\text{dBm}] - 3[\text{dB}] &= IP3_{IN}[\text{dBm}] - \frac{|R_{SFDR}[\text{dB}]| - 3[\text{dB}]|}{2} - |G_{PD}[\text{dB}]| \\ \Rightarrow P_{RF}[\text{dBm}] &< IP3_{IN}[\text{dBm}] - \frac{|R_{SFDR}[\text{dB}]|}{2} - |G_{PD}[\text{dB}]| + 1.5[\text{dB}] \end{aligned} \tag{40}$$

Where R_{SFDR} is the SFDR at the IF port due to a given RF port power. An additional 3 dB is also subtracted such that P_{RF} may be used to represent the power in the entire signal. This is merited by the fact that FM signals have constant power. Note that this is a worst-case limit. An accurate analysis is made complicated by the fact that both the number of individual components, as well as their power vary with modulation index. The phase of the components is neither constant.

The last matter to consider is the amplitude noise at the IF port. This is characterized by the noise figure of the mixer. The noise figure can be rewritten to obtain the relation between input noise at the RF port, to output noise at the IF port.

$$F_{PD} = \frac{\left(\frac{P_{RF}}{N_{RF}}\right)}{\left(\frac{P_{IF}}{N_{IF}}\right)} = \frac{N_{IF}}{N_{RF}}\frac{P_{RF}}{P_{IF}} \Rightarrow N_{IF} = \frac{F_{PD}N_{RF}P_{IF}}{P_{RF}} = \frac{F_{PD}N_{RF}P_{RF}G_{PD}}{P_{RF}} = G_{PD}F_{PD}N_{RF} \tag{41}$$

Where N_{IF} and N_{RF} is the noise power at the IF and RF port respectively, F_{PD} is the mixer single side band noise figure and, P_{IF} and P_{RF} is the signal power at the IF and RF port respectively.

Now that expressions have been found for the requirements imposed on the RF port power as well as the gain of IF amplifier, consider the PLL's transfer function in the frequency domain. Taking the derivative of the output voltage, described by Equation 22, around its operating point yields

$$\frac{dV_{IF}\left(\pm\frac{\pi}{2}\right)}{d\Delta\phi} = \frac{d}{d\Delta\phi}\sqrt{2G_{PD}P_{RF}R}\cos(\Delta\phi) = -\sqrt{2G_{PD}P_{RF}R}\sin\left(\pm\frac{\pi}{2}\right) = \mp\sqrt{2G_{PD}P_{RF}R} \tag{42}$$

In practice, the polarity of the gain depends on how the double balanced mixer is internally coupled. Even though the IF port is inherently balanced, it commonly has one of the balanced lines internally tied to ground. Depending on which line is grounded, the mixer either has positive or negative gain. Whether positive or negative is desired depends on the loop filter. Let's define positive gain as when an increase at the input RF port gives an increase at the output IF port. Then, a phase detector with positive gain is described by

$$V_{IF} = 2\left|\frac{dV_{IF}\left(\pm\frac{\pi}{2}\right)}{d\Delta\phi}\right|(\phi_{RF} - \phi_{LO}) = 2\sqrt{2G_{PD}P_{RF}R}(\phi_{RF} - \phi_{LO}) = K_{PD}(\phi_{RF} - \phi_{LO}) \quad (43)$$

Where a factor two is added such that the output resistance of the IF port may be modelled. The schematic representation is then a summation block, gain block with gain K_{PD}, and a series 50 Ω resistor, in that order.

To summarize, the mixer imposes two conditions on the surrounding circuitry. First, for a given SFDR, there must be an amplifier at the IF port with a gain satisfying the limit given by Equation 36. An approximation of the required loop gain in terms of amplitude ripple can also be found in Equation 30. Second, the RF port power must be less than that given by Equation 40, also to obtain a given SFDR.

An expression for the phase detector's transfer function is given by Equation 43, where it is assumed that the RF port is used as input and that the mixer has positive gain.

2.3.2.3 The Loop Filter

The loop filter is positioned at the output of the phase detector and serves three main purposes. It low pass filters the signal, removing the upper sideband at two times the center frequency. Furthermore, it has high gain to let the phase detector work with small signals and as such, in a linear fashion. Additionally, and most importantly, it has a transfer function intended to stabilize the loop.

This thesis only considers two types of filters, constant gain (with low pass filtering) and integrator type response with amplifiers in open loop. The noise gain for these different filters are analyzed in section 2.3.2.1 and the latter is assumed the better candidate because of its decreased cost.

From a requirements point of view, the amplifiers must have sufficient slew rate to handle the desired signal levels. By considering the derivative of a sinusoidal, and evaluating at its largest value, the frequency must satisfy

$$f_m \leq \frac{S_R}{2\pi \cdot \max\{\hat{V}_m\}} \quad (44)$$

Where S_R is the slew rate. Other figure of merits to consider are noise levels and unity gain bandwidth.

2.3.2.4 The Voltage Controlled Oscillator

A brief description of the VCO, and how it is used to synthesize the FM signal, is given in 2.3.1. Here, its ideal transfer function is presented.

Since the transfer function of the phase detector is naturally expressed in terms of input phases, the same is done for the VCO. Equation 8 describes the output signal in the time-domain. Its phase is given by the argument of the sine term. The phase may be expressed in the s-domain as

$$\phi_{out}(s) = \mathfrak{L}\left\{\omega_0 t + 2\pi K_{VCO}\int_0^t V_m(t)dt\right\} = \frac{\omega_0}{s} + 2\pi K_{VCO}\frac{V_m(s)}{s} \tag{45}$$

Since the PLL compares two signals with equal center frequency, and the phase detector's output is proportional to $\phi_1 - \phi_2$, the leftmost term can be ignored when the loop is locked. The relation then simplifies to

$$\frac{\phi_{out}(s)}{V_m(s)} = \frac{2\pi K_{VCO}}{s} \tag{46}$$

If the VCO is used at high modulating frequencies, it is also necessary to account for parasitic impedances at its input. Inclusion of a transfer function describing theseyields

$$\phi_{out}(s) = G_{VCO}(s)\frac{2\pi K_{vco}}{s}V_m(s) \tag{47}$$

Where G_{VCO} models the parasitic impedance network at the VCO input.

It should be restated that since the modulating voltage is large, the voltage to frequency relationship is not linear. This, as mentioned in the beginning of Section 2.3, matters less if the same VCO is used in both modulator and demodulator. The analysis given in [2] supports this statement.

2.3.2.5 Propagation Delay

As the length of the feedback loop in the PLL is not insignificant, the propagation delay of the signal must be accounted for. The propagation delay causes phase shifts which ultimately affect the stability of the loop. The delay is simply the pathlength divided by the speed of the signal.

$$t_d = \frac{L_p\sqrt{\epsilon_r}}{c_0} \tag{48}$$

Where L_P is the pathlength of the feedback loop, c_0 is the speed of light in vacuum and ϵ_r is the effective relative permittivity. In the s-domain, the delay can be expressed by the following transfer function,

$$G_d(s) = e^{-st_d} = e^{-s\frac{L_p\sqrt{\epsilon_r}}{c_0}} \tag{49}$$

The function may be inserted anywhere in the loop if accurate phase at points within the loop is not required. Do note that the delay will cause significant phase shift at higher frequencies.

2.3.2.6 Noise Considerations

In the design process, it is assumed that only amplitude noise is of interest. The real reason is that an analysis of phase noise would require knowledge of the phase noise generated by each part of the transmission chain. This is unknown. The secondary reason is that since the signal will typically be output to an oscilloscope, frequency jitter will not be visible unless large time ranges are used. It is then only a problem if several measurements need to be synced. Furthermore, it is assumed that indirect amplitude noise contributions from phase noise is negligible compared to other noise sources.

To remove the amplitude noise present on the PLL input, the signal is first passed to a limiting amplifier and it is assumed that it attenuates the noise to negligible levels. After the limiter, the signal is attenuated to conform with the spur requirements imposed by the intermodulation products of the phase detector. To make the signal of both reference VCO and modulating VCO similar, the reference VCO is also amplitude limited.

2.3.2.7 Summary

Equation 36 and 30 gives a lower limit for the loop gain. The latter can be used to estimate the required gain for a stable loop and the aforementioned determines the necessary gain for a given SFDR.

Since both Equation 14 and 44 describes an upper frequency limit, and are inversely related to the peak modulating voltage, there exist an optimum voltage where the frequency range is maximized. This is likely a value much larger than is realizable and instead, the peak modulating voltage can be calculated directly from the slew rate limited value given by Equation 44.

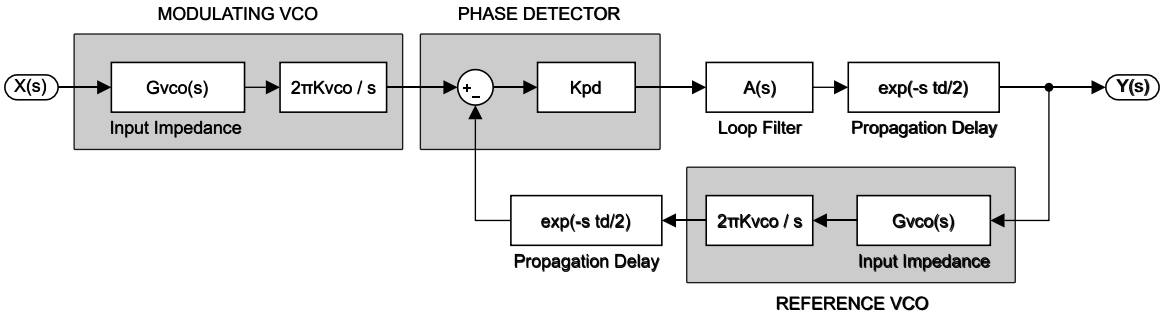

Figure 6 – Simulation model of the phase-locked loop and the modulating VCO under consideration.

The complete simulation model can be seen in Figure 6. The propagation delay is described by Equation 48, the phase detector is modelled by Equation 43 and, the VCO by Equation 47. The loop filter is not described as it would have to incorporate parasitic components which are better obtained through simulations.

2.3.3 Transmission of DC Level Signals

In theory, FM modulation is well suited for the transmission of DC and very low frequency signals. However, the VCO has significant temperature drift. For example, the HMC385 from Analog Devices can drift as much as 40 MHz over its temperature range, when it is biased at 5 V. When demodulated by the reference VCO, the voltage error may be as large as 1 V. As such, if DC levels must be maintained, it is necessary to control the drift in some manner. Possible solutions include temperature control, feedback output center frequency to affect the bias voltage or, send the DC signal by other means (e.g. sampling). Of these, the latter is assumed to have the best cost – performance ratio.

2.4 Estimation of Parasitic Impedances

To estimate the parasitic impedance associated with a component pad, the pads can be considered as microstrips. The capacitance and inductance of a microstrip line can be approximated by [7]

$$\begin{aligned} L &\approx 2 \cdot 10^{-7} \ln\left(\frac{5.98h}{0.8w + t}\right) \\ C &\approx \frac{2.64 \cdot 10^{-11}(\epsilon_r + 1.41)}{\ln\left(\frac{5.98h}{0.8w + t}\right)} \end{aligned} \tag{50}$$

Where L is the inductance per meter (H/m), C is the capacitance (F/m), w is the width of the trace, h is the thickness of the dielectric, t is the thickness of the copper and ϵ_r is the relative permittivity of the material. The approximation is valid for moderate to small w/h ratios. From the examples listed in [8], it is assumed that the formula is valid for w/h < 3.

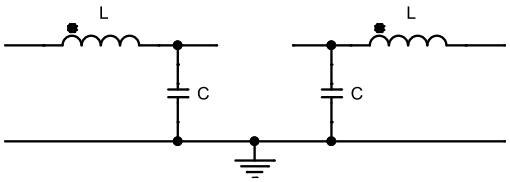

Figure 7 – Modelling the parasitic impedance associated with the footprint of a passive element.

By approximating a component pad as a length of microstrip, the model given in Figure 7 may be used to approximate the parasitic impedance associated with the pad itself. L and C is obtained by inserting the pad width into Equation 50 and then multiplying with the length of the pad.

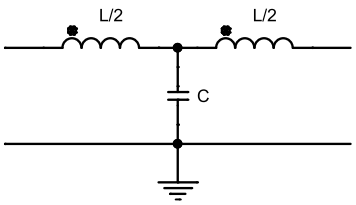

Figure 8 – Modelling a small length of transmission line.

Figure 8 shows the approximation of a small length of transmission line interconnecting two components. L and C is obtained either directly from Equation 50 or by the characteristic impedance relation $Z_0 = \sqrt{L/C}$.

Additionally, if the width of the trace interconnecting two elements is not equal that of the pad it connects to, there will be an additional impedance associated with the

discontinuity. This effect, however, can be omitted by simply interconnecting components with the same trace width as that of the pads.

Chapter 3
Implementation

The proposed system consists of a battery powered sensor head and a line driven receiver. The sensor head is connected to the measurement node by a balanced cable. Because of DC drift, the measured signal is split into two paths, a low frequency path and high frequency path. The high frequency path is frequency modulated and transmitted over an analog optical link to the receiver, where it is demodulated by a phase locked loop. The low frequency path is digital and transmitted over a low speed optical link. At the receiver, it is reconverted and joined with the high-speed path at the output. The output is thus analog and may be connected to, for example, an oscilloscope.

In this section, the design of the sensor head, and how it limits common mode interference, is elaborated upon. Furthermore, the previously derived theory is used to determine design parameters for the different blocks in the signal chain. Details on surrounding circuitry is only considered in passing.

3.1 Sensor Head

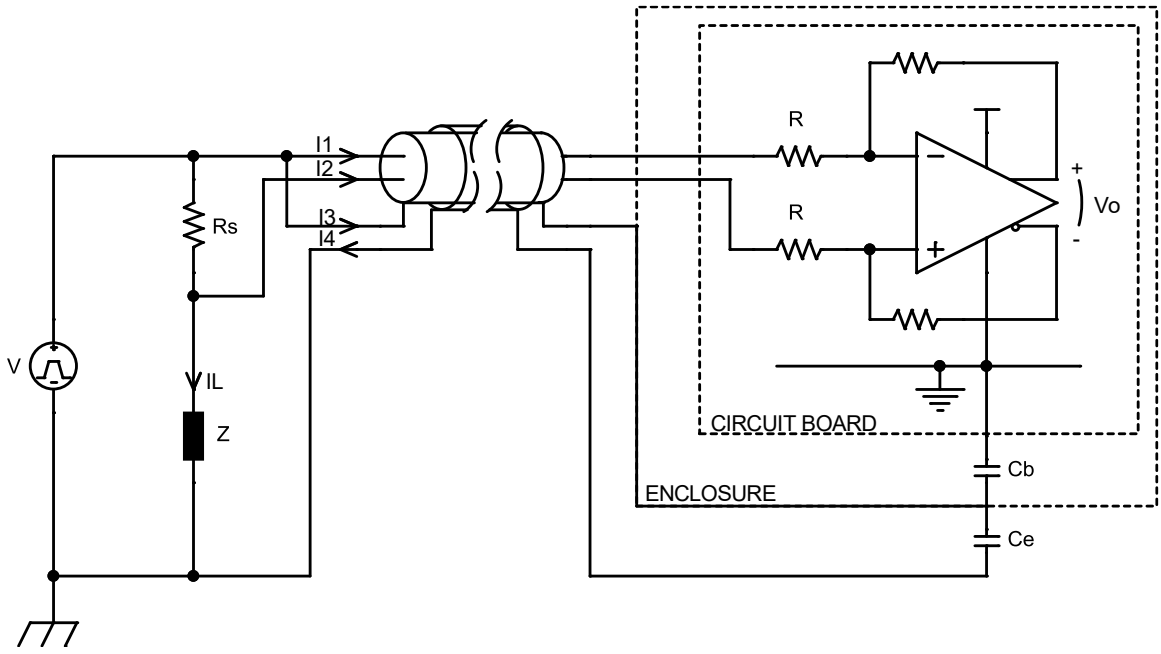

Figure 9 – Illustration of how the input stage is designed to minimize common mode errors.

The sensor head and how its design is intended to limit common mode interference will here be considered in the view of a current shunt. This is just one example from the range of applications but represents a typical one.

Consider the measurement setup illustrated in Figure 9. C_e represents the capacitive coupling between enclosure and measurement object, and C_b, the capacitive coupling between the enclosure and the circuit board inside of it. A shielded balanced cable is connected to the current shunt, R_S. The cable shield is connected to one side of the shunt to bring the potential of the enclosure, enclosing the measurement apparatus, close to that of the current shunt. That way, the bulk of the common mode current flows through the shield instead of the balanced wires, which carries the signal. If the shield has zero impedance, it means that the measurement error is minimized. To account for non-zero shield impedance, an additional shield is shown around the cable. This is simply to illustrate the fact that the common mode current flowing through the shield senses an impedance which is dependent on how close the cable is to whatever object is carrying the return current.

To determine a model of the system, certain approximations are made. For instance, the cable is assumed to be less than 30 cm. This means that a single inductance is a fair approximation of the return path / shield impedance, for frequencies less than 100 MHz. It is also assumed that the current flowing through the shield will couple fully to the

balanced pair and that the wires constituting the pair couples fully to each other. Furthermore, the coupling between enclosure and return path is considered a single capacitance. The prototype enclosure has a side length of about 10 cm and by comparison to a monopole antenna, this corresponds to a resonance frequency of 750 MHz. It is then likely that for frequencies less than 100 MHz, a capacitance is a reasonable approximation. The approximations lead to the circuit model shown in Figure 10. The mutual inductance, and self-inductance, of the shield and balanced pair is assumed to be equal, because they share the same external magnetic field.

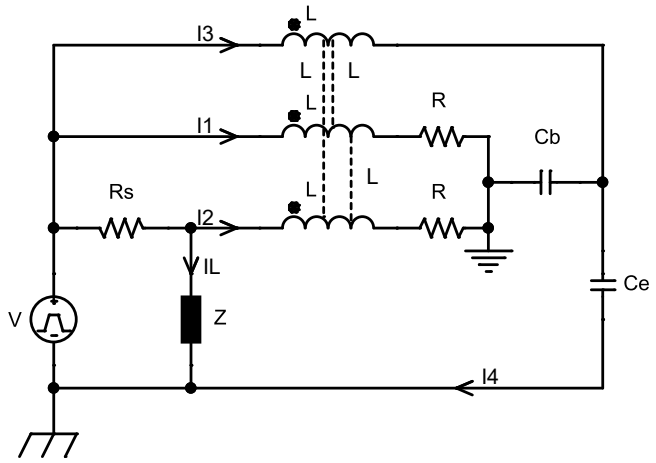

Figure 10 – Circuit model of the illustration in Figure 9.

Node analysis give the following expression for the differential mode voltage the amplifier senses.

$$\begin{aligned} V_{DM}(s) &= I_1 R - I_2 R \\ &= sL(I_1 + I_2 + I_3) - sL(I_1 + I_2 + I_3) - V_{C_b} \\ &- \left(sL(I_1 + I_2 + I_3) - sL(I_1 + I_2 + I_3) - V_{C_b} - V_{R_s}\right) = V_{R_s} \end{aligned} \tag{51}$$

By solving the equation system representing the circuit and dividing the differential mode voltage with the expected voltage, a representation of the differential error is obtained. The expression should be equal to 1.

$$\frac{V_{DM}(s)}{I_L R_s} = \frac{R(sC_b R + 2)}{2R + R_s + sC_b R^2 + sC_b R R_s} \approx \frac{R(sC_b R + 2)}{2R + sC_b R^2} = 1 \tag{52}$$

Where the approximation is valid for $R \gg R_S$. It is seen that there is no differential error as long as the shunt resistance is much lower than the input resistance of the amplifier.

The common mode voltage the amplifier senses is

$$
\begin{aligned}
V_{CM}(s) = \frac{I_1 R + I_2 R}{2} &= \frac{\begin{array}{c} sL(I_1 + I_2 + I_3) - sL(I_1 + I_2 + I_3) - V_{C_b} + \\ + \left(sL(I_1 + I_2 + I_3) - sL(I_1 + I_2 + I_3) - V_{C_b} - V_{R_s}\right) \end{array}}{2} \\
&= -\left(V_{C_b} + \frac{V_{R_s}}{2}\right) \\
&= -\frac{C_b R^2 R_s s\, V}{2\,(2RR_s + 2RZ + R_s Z + C_b R^2 R_s s\ + C_b R^2 Z s + C_b R\, R_s Z s)} \\
&\approx -\frac{C_b R^2 R_s s\, V}{2\,(2RZ + sC_b R^2 Z)} = -\frac{V}{Z}\frac{R_s}{2}\frac{s\frac{RC_b}{2}}{1 + s\frac{RC_b}{2}} \approx -\frac{I_L R_s}{2}\frac{s\frac{RC_b}{2}}{1 + s\frac{RC_b}{2}} \\
&\to -\frac{I_L R_s}{2} \text{ as } s \to \infty
\end{aligned}
\tag{53}
$$

Where the approximation is valid for $|Z| \gg R_S$, $R \gg R_S$. The common mode voltage is seen to be independent of both C_e and L. It means that how well the system rejects common mode voltages is independent of how the sensor head is spatially placed in relation to the measurement object. It does, however, not mean that its placement can be disregarded. While the current that flows through the shield does not affect the measurement, it is still drawn from the source. As the cable and sensor head radiates in proportion to the current drawn, minimizing the current is of interest. Furthermore, shield resistance, and inductance in the shield connection at the measurement object, will cause voltage drops which will not cancel like the inductively coupled voltages did. This is not accounted for in the model.

If high input impedance is necessary, resistances may be connected in series with the balanced pair at the measurement node. This do degrade the SNR of the measurement itself and may or may not be possible for a given setup.

3.2 Signal Chain

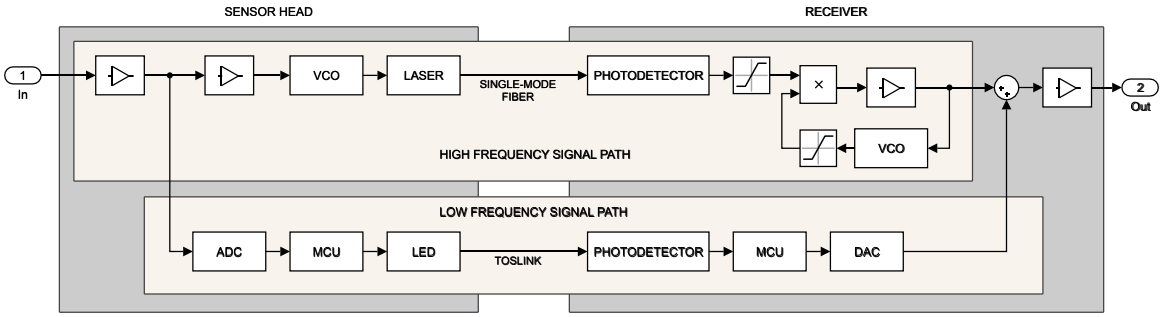

Figure 11 – Block representation of the full signal chain.

Following is a brief description of the implementation of the signal chain. Requirements derived in the theory section are used to justify design choices and to obtain simulation model parameters. It is the intent to design a system with as high performance as possible and as such, design parameters are mostly made to fit the available components and not its reverse. There are, of course, fundamental requirements which must be fulfilled. First, the system should be able to measure voltages on current shunts. These are approximately 20 mV full scale. Second, it must be able to handle DC to 100 MHz. Lastly, the minimum dynamic range must be at least 40 dB. No hard value is given for the spurious free dynamic range, but it should preferable be greater than 40 dB as well.

The signal chain is implemented by separating the input into a high frequency analog path and a low frequency digital path. This is necessary because the high frequency path has severe DC drift. Both paths are joined before being output to the external measurement instrument. A digital filter smooths the transition between the DC coupled low frequency path and the AC coupled high frequency path.

In the high frequency path, the signal is frequency modulated and transmitted over an optical fiber. Following the receiving photodiode, the FM signal is demodulated by a PLL. The low frequency path is digital, where the input is sampled and sent over a low speed optical data link.

3.2.1 Frequency Signal Chain

3.2.1.1 Obtaining Block Requirements

It is appropriate to begin the design process by considering the components where the selection is limited. As such, consider the optical transmission chain.

AFBR-1310Z and AFBR-2310Z from Avago Technologies constitutes a matched laser – photodiode pair which implements a black box solution. The pair has internal RF amplifier circuitry and accepts a frequency range of 200 MHz to 5.5 GHz. Furthermore, the laser has an already pre-aligned pigtail and is thus convenient to use. The guaranteed optical power is specified as 5 mW over its operating temperature range which limits the electrical input power according to

$$\begin{aligned} P_{opt} = 20\left[\frac{mW}{V}\right]V_{el} \Leftrightarrow \frac{P_{opt}^2}{50[\Omega]\left(20\left[\frac{mW}{V}\right]\right)^2} = \frac{V_{el}^2}{50[\Omega]} = P_{el} \\ \Rightarrow P_{el} < \frac{(5\ [mW])^2}{50[\Omega]\cdot\left(20\left[\frac{mW}{V}\right]\right)^2} = 1.3\ mW = 0.96\ dBm \end{aligned} \tag{54}$$

Where P_{opt} and V_{el} is the laser optical output power and input voltage respectively. The voltage to power gain is taken from the data sheet. As the laser is tied to the input of the VCO, Equation 54 also describes the power requirement imposed on the VCO.

It is also necessary to ascertain the SNR at the photodiode output. The laser figure of merit, relative intensity noise, RIN, is the inverse of the (electrical) SNR at the photo detector output divided by the system bandwidth, while assuming the photodetector does not contribute noise [9].

$$S_{PHD} = \frac{1}{BR_{IN}} = \frac{1}{10^{-\frac{120}{10}}\left[\frac{1}{Hz}\right]\cdot B} = 10^{12}[Hz]\cdot\frac{1}{B} \tag{55}$$

Where R_{IN} is the relative intensity noise of the laser (obtained from the data sheet), S_{PHD} the laser associated SNR at the output of the photodetector and B, the bandwidth. The photodiode, AFBR-2310Z, has an internal amplifier. If the amplifier is assumed noiseless, the RIN specified for the laser is also the SNR at the output from the photodiode. By knowledge of the photodetector output power, the noise can be obtained. For an incoming optical power of 5 mW, the output power noise is,

$$S_{PHD} = \frac{P_{PHD}}{N_{PHD}}$$
$$\Rightarrow N_{PHD} = \frac{P_{HD}}{S_{PHD}} = P_{PHD} B R_{IN} = \frac{\left(200\left[\frac{V}{W}\right] 5[mW]\right)^2}{50[\Omega]} \cdot 10^{-12}\left[\frac{1}{Hz}\right] \cdot B \qquad (56)$$
$$= 2 \cdot 10^{-14}\left[\frac{W}{Hz}\right] \cdot B$$

Where P_{PHD} and N_{PHD} is the signal power and noise power respectively. The optical power to electrical output gain is obtained from the data sheet of the photo detector. The noise generated by the photodiode itself is, by figures from its datasheet,

$$\frac{\left(10\left[\frac{pW}{\sqrt{Hz}}\right] \cdot \sqrt{B} \cdot 200\left[\frac{V}{W}\right]\right)^2}{50[\Omega]} = 8 \cdot 10^{-20}\left[\frac{W}{Hz}\right] \cdot B \qquad (57)$$

Which is seen to be much less than the noise generated by the laser and can be omitted. The signal to noise ratio is then simply as given in Equation 55. For a bandwidth of 372 MHz, the CNR is 34.3 dB. The bandwidth is the bandwidth of the FM signal and is calculated in Equation 63.

As for choice of VCO, there are two key points which must be considered. First, the input port impedance must be such that it does not limit the input frequency. Secondly, it must have a wide voltage tuning range to allow for large modulation indexes. HMC385 from Analog Devices is a suitable choice as the input impedance is well specified and given a 50Ω source, has a corner frequency of 60 MHz. This can be improved if needed by lowering the source impedance while keeping transmission line length short. Its tuning range is 11 V and thus accepts large modulating amplitudes, $\widehat{V}_m$. From the datasheet, at a bias voltage of 5 V, the VCO gain is K_{VCO} = 40 MHz/V. At this bias voltage, the center frequency is 2.45 GHz.

To obtain a suitable modulating voltage, it is necessary to consider the amplifiers in the loop filter. These will either be slew rate limited, limited by output voltage swing or limited by distortion. The chosen amplifier is AD8099 from Analog Devices. It has a slew rate of 1350V/μs, an output voltage swing of 7 V with 10 V supply and, an SFDR greater than 40 dB for frequencies less than 100 MHz. In addition, it has a unity gain frequency of 3.8 GHz.

By Equation 44, at a modulating frequency of 100 MHz, the peak modulating voltage should be 2.14 V.

$$f_m = \frac{S_R}{2\pi \cdot \max\{\hat{V}_m\}} = \frac{1350\left[\frac{\mu s}{V}\right]}{2\pi \cdot 2.14[V]} = 100\ \text{MHz} \tag{58}$$

The choice of phase detector is made on the basis of frequency range and IP3 product. It is of interest to have as high RF port power as possible and this requires a high IP3 product. Phase detectors from Analog Devices have mainly been considered and of the available choices, only HMC213A satisfies the bandwidth and center frequency requirements imposed by the VCO. At the center frequency, 2.45 GHz, with an LO power of 15 dBm, the input referred IP3 product is approximately 20 dBm and the conversion gain is approximately -8 dB. Then, from Equation 40, the RF port power must be less than -6.5 dBm according to

$$\begin{aligned} P_{RF}[\text{dBm}] &< IP3_{IN}[\text{dBm}] - \frac{|R_{SFDR}[\text{dB}]|}{2} - |G_{PD}[\text{dB}]| + 1.5[\text{dB}] \\ &= 20[\text{dBm}] - \frac{40[\text{dB}]}{2} - 8[\text{dB}] + 1.5[\text{dB}] = -6.5\ \text{dBm} = 223\ \mu\text{W} \end{aligned} \tag{59}$$

Where the SFDR is set to 40 dB and G_{PD} and the IP3 rating is obtained from the phase detector's datasheet. The minimum loop filter gain for a given SFDR is given by Equation 36

$$\begin{aligned} A_{V,IF} &> \max\{\hat{V}_m\}\sqrt{\frac{3 \cdot R_{SFDR}}{48 \cdot RP_{RF}G_{PD}}} = 2.14[V]\sqrt{\frac{3 \cdot 10^{\frac{40}{20}}}{48 \cdot 50[\Omega] \cdot 223[\mu W] \cdot 10^{-\frac{8}{10}}}} = 127 \\ &= 42\ \text{dB} \end{aligned} \tag{60}$$

If the loop filter has a fixed gain, Equation 30 states that the loop filter gain must be greater than

$$\begin{aligned} A_{V,IF} &\geq \frac{f_m}{R_\sigma K_{VCO}\sqrt{2G_{PD}P_{RF}R}} = \frac{100\ [\text{MHz}]}{4[\%] \cdot 40\left[\frac{\text{MHz}}{V}\right]\sqrt{10^{-\left(\frac{8}{10}\right)} \cdot 223[\mu W] \cdot 50[\Omega]}} \\ &= 1049 = 60.4\ \text{dB} \end{aligned} \tag{61}$$

Where the accuracy is set to 4 %, corresponding to a 0.5 dB amplitude deviation.

To minimize the noise at the input, the signal applied to it is first passed to a limiting amplifier. The amplifier will reject AM noise while preserving the signal spectrum. A fixed gain block from Texas Instruments, TRF37C75, is chosen on merits of its relatively flat passband and small form factor. At 2.45 GHz, its gain is 17.2 dB. With an output referred

compression point of 18 dBm, the photodetector can easily drive the gain block into saturation. The photodetector output power is given equal to

$$P_{PHD} = \frac{\left(5[\mathrm{mW}] \cdot 200\left[\frac{\mathrm{V}}{\mathrm{W}}\right]\right)^2}{50} = 20\mathrm{mW} = 13\mathrm{dBm} \tag{62}$$

At the output of the gain block, the signal needs to be attenuated to conform with the limit on the phase detector RF port power, -6.5 dBm. The output power from the gain block is 18 dBm, since it is saturated, and inserting two fixed attenuation blocks, Susumu PAT1220, after the amplifier will be sufficient to match the levels.

Equation 15 is used to verify that the optical transmission chain has sufficient bandwidth,

$$B < 2\left(K_{vco} \cdot \max\{\hat{V}_m\} + \max\{f_m\}\right) = 2\left(40\left[\frac{\mathrm{MHz}}{\mathrm{V}}\right] \cdot 2.14[\mathrm{V}] + 100[\mathrm{MHz}]\right) = 372\ \mathrm{MHz} \tag{63}$$

Which is considerably less than the bandwidth of the optical connection. However, it is still large enough such that a flat passband cannot be assumed. As mentioned earlier, if the paths at the outputs of both the VCO in the PLL and that of the transmitter, are not identical, distortion results. Whether or not this is a problem is not considered due to the complexity of setting up an analysis of the RF signal chain.

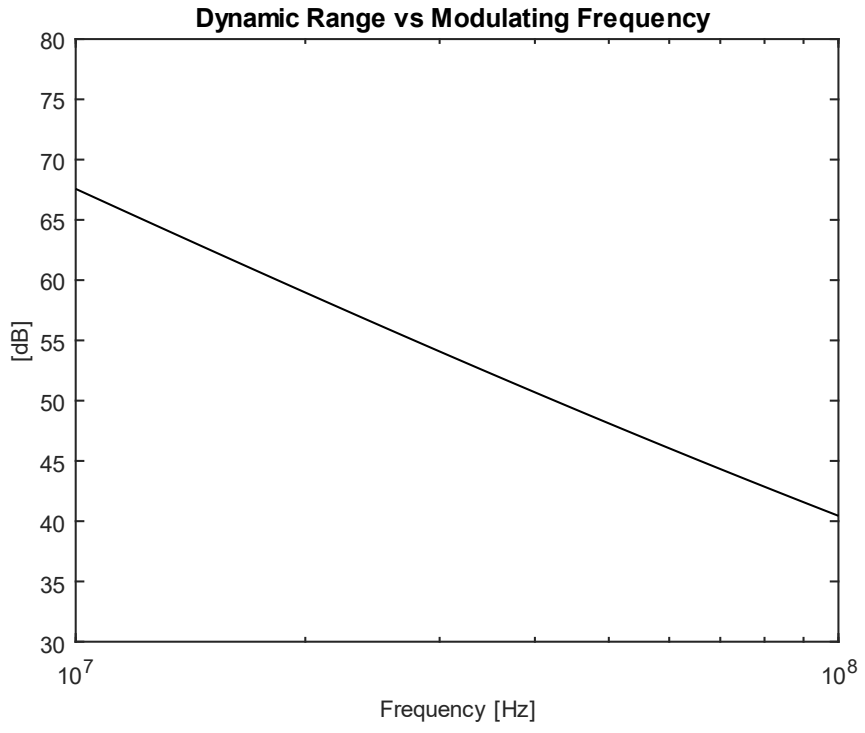

Figure 12 – Dynamic range as predicted by Equation 12.

With the values obtained from this section, the dynamic range as predicted by Equation 12 is plotted in Figure 12. The signal chain noise floor will limit the dynamic range for lower frequencies. Other results obtained in this section can be summarized in the following tables

Table 1 – Summary of derived block parameters.

max{f_m}	100 MHz
max{$\hat{V}_m$}	2.14V
P_{RF}	-6.5 dBm
min{SFDR}	40 dB
min{$A_{V,IF}$} for the given SFDR	42 dB
min{$A_{V,IF}$} for stability at fixed gain	60.4 dB
Accuracy, $R_\circ$ at fixed gain	4 % ≈ 0.5 dB
CNR at photodiode output	34.3 dB

Where the following components are chosen

Table 2 – Summary of chosen components.

RF Gain block	TRF37C75
RF Attenuator block	PAT1220
Loop Amplifier	AD8099
Phase detector	HMC213A or HMC213B
VCO	HMC385
Laser	AFBR-1310Z
Photo detector	AFBR-2310Z

3.2.1.2 The Loop Filter

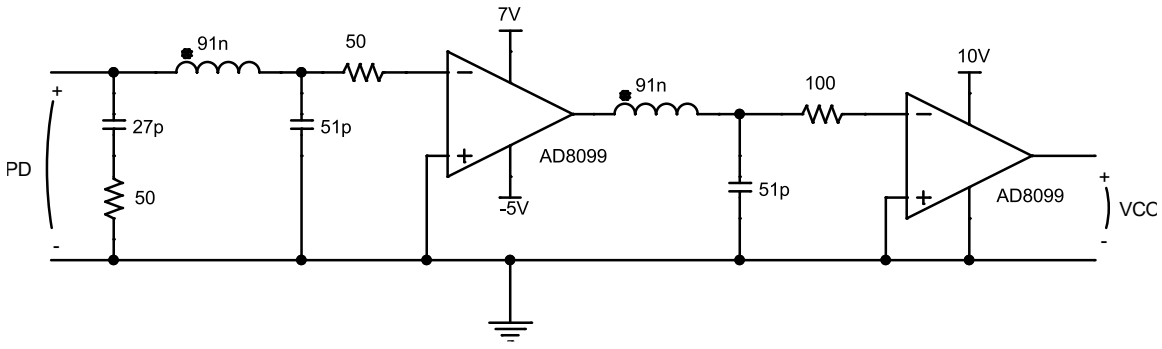

Figure 13 – The loop filter.

Both loop amplifiers are configured in open loop in accordance to the reasoning given in Section 2.3.2.1. While other filter structures exist that are intended to improve loop stability, these are unnecessary in this case as the raw gain of two amplifiers is sufficient to stabilize the loop. As shown in Section 2.3.2.1, the noise gain is neither adversely affected as opposed to having fixed gain. Considering the increased simplicity, and decreased cost from not having to use expensive RF resistors, open loop configured amplifiers seems like an appropriate choice.

The resistor and capacitor at the input to the first amplifier matches the impedance to the phase detector IF port at radio frequencies. This is necessary not only because of power loss but because signals reflected back onto the mixer will be mixed and re-emitted, causing distortion. The LC filter at the input to each amplifier filters out the twice RF frequency produced by the phase detector, limits noise by low pass filtering and, stabilizes the loop.

3.2.1.3 Obtaining Simulation Parameters

To simulate the signal chain, it is necessary to obtain the parameters from the previously derived equations. The phase detector model is, from Equation 43,

$$\begin{aligned} V_{IF} = K_{PD}(\phi_{RF} - \phi_{LO}) &= 2\sqrt{2G_{PD}P_{RF}R}(\phi_{RF} - \phi_{LO}) \\ &= 2\sqrt{2 \cdot 0.1585 \cdot 223[\mu W] \cdot 50[\Omega]}(\phi_{RF} - \phi_{LO}) \\ &= 0.12[V] \cdot (\phi_{RF} - \phi_{LO}) \end{aligned} \tag{64}$$

The VCO model is obtained from Equation 47, together with figures from its datasheet [10]. At a bias voltage of 5 V,

$$\phi_{out} = \frac{G_{VCO}(s)}{s} 2\pi \cdot K_{vco} V_{mod} = \frac{G_{VCO}(s)}{s} 2\pi \cdot 40 \left[\frac{MHz}{V}\right] V_{mod}(s) \tag{65}$$

Where the VCO input impedance is given by $G_{VCO}(s)$ and can be found in the datasheet [10].

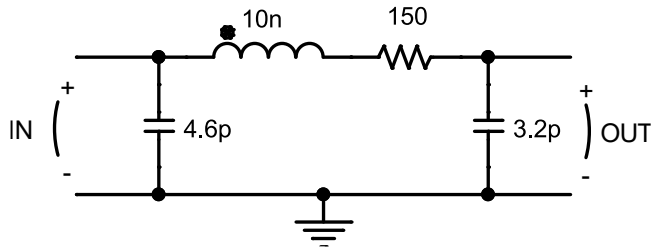

Figure 14 – VCO input impedance as given by the datasheet [10].

Where the output is to be connected to the ideal integrator.

Equation 48 is used to estimate the propagation delay. The actual pathlength, L_p, is taken from the finished layout and is equal to 73 mm. The effective permittivity can only be approximated because the signal propagates both through integrated circuits as well as through passive filter chains with varying structure due to component pads. Limits can however be obtained by considering the signal propagating either entirely through air, or entirely through the dielectric. Inserting a value for the relative permittivity of 4.2 and 1 for the dielectric and air respectively, into Equation 48, yields the delay limits.

$$t_d = \frac{L_p\sqrt{\epsilon_r}}{c_0} = \frac{73[\text{mm}]}{300 \cdot 10^6 \left[\frac{\text{m}}{\text{s}}\right]}\sqrt{\epsilon_r} \in \{243\text{ps}, 500\text{ps}\}\} \tag{66}$$

A realistic value is probably on the upper end, and for simulations, a delay of 400 ps is assumed. To give an idea of the order of the delay, at a frequency of 200 MHz, the phase shift is 28.8 degrees. Note that the delay can be improved by considering the transmission line structure. As the spacing between signal traces and top ground decreases, the part of the signal energy which propagates through air increases, thus lowering the effective relative permittivity and as a result, lowers the delay.

To ascertain how much noise is generated at the system output if the photo detector is applied directly to the phase detector RF port, and as such if the limiting amplifiers may be omitted, calculate the open loop noise at the IF port due to the phase detector and its inputs. Insert Equation 56 into Equation 41,

$$N_{IF} = N_{PHD}G_{PD}F_{PD} = 2 \cdot 10^{-14}\left[\frac{\text{W}}{\text{Hz}}\right] \cdot B \cdot G_{PD}F_{PD} \tag{67}$$

Which can be modelled as a resistor by converting the noise to voltage and equating to the thermal noise of an ideal resistor.

$$\begin{aligned}\sqrt{50[\Omega]\cdot N_{IF}} = \sqrt{4kTBR} \Leftrightarrow 50[\Omega]\cdot N_{IF} = 4kTBR \\ \Rightarrow R = \frac{50[\Omega]}{4kTB}\cdot N_{IF} = \frac{50[\Omega]}{4kTB} N_{PHD} G_{PD} F_{PD} \\ = \frac{50[\Omega]}{4\cdot 1.38\cdot 10^{-23}\left[\frac{J}{K}\right]\cdot 300[K]\cdot B}\cdot 2\cdot 10^{-14}\left[\frac{W}{Hz}\right]\cdot B\cdot 10^{-\frac{8}{10}} 10^{\frac{8.5}{10}} \\ = 68\ M\Omega\end{aligned} \quad (68)$$

Since this is the noise present in an equivalent high impedance resistor in parallel with the 50 Ω IF output resistor, it must be isolated from the rest of the circuit. If inserted in series with the summation- and gain block of the phase detector, the resistance should be multiplied by two because of voltage division between IF port impedance and its load.

3.2.2 Low Frequency Signal Chain

The low frequency signal chain is fully digital and made up of an ADC at the sensor head and a DAC at the receiver. The digitized signal is sent over a low speed optical data link. Since the dynamic range of the high-speed chain is less than 60 dB, the requirements on the resolution are quite relaxed. A 10 bit resolution is sufficient. As such, the integrated 16-bit ADC and 10-bit DAC of the microcontroller PIC24FJ128GC010 from Microchip is used as it is both cost-effective and has a small form factor. If necessary, the DAC resolution may be increased by data processing techniques.

Since the data rate is low, most optical data links may be used. Here, GP1FAC31T0OF and GP1FAV31RK0F from Sharp is chosen. It is a TOSLINK pair and the plastic fibers necessary for its interconnection are inexpensive as they are used in common multimedia equipment.

3.2.3 Input Stage

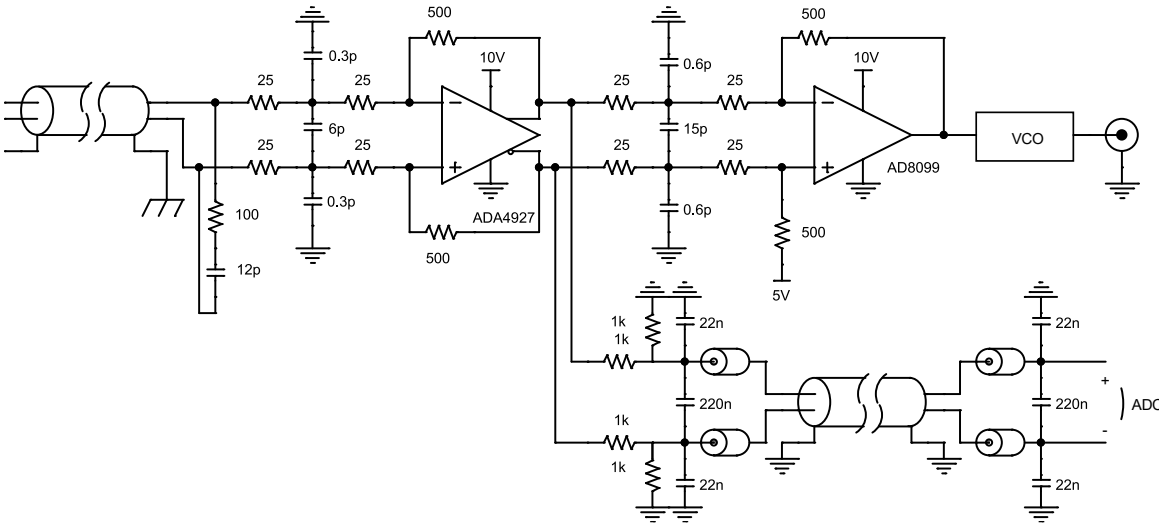

Figure 15 – Simplified schematic of the input stage and its connection to the measurement node.

The signal to be measured is connected to the sensor head by a balanced 100 Ω twin axial cable, Belden 9207 with matching connectors Amphenol 162100/162103. To amplify the signal, the differential amplifier ADA4927 from Analog Devices is chosen on merits of its low distortion (> 70 dBc for f < 100 MHz), and noise (1.3 nV/$\sqrt{\text{Hz}}$). The reason for choosing a differential amplifier is that the ADC is placed on a separate circuit board and differential signaling improves rejection to disturbances. Since a cable is interconnecting the two points, there are common mode filters at each end to make sure that noise coupled onto the cable is low pass filtered. They also serve as aliasing filters.

At the output of the differential amplifier, the same type of amplifier used in the loop filter, AD8099, converts the signal to single ended as required by the VCO. The desired total gain of the stages is given by

$$A_{V,INPUT} = \frac{\max\{\hat{V}_{mod}\}}{\max\{\hat{V}_{input}\}} = \frac{2.14[V]}{20[mV] \cdot \sqrt{2}} = 37.6\ dB \tag{69}$$

Where the measured signal is 20 mV RMS full scale.

Each amplifier has a common mode and differential filter that is made part of their gain resistor network. The input amplifier also has an extra 100Ω + 12 pF added for impedance matching.

3.2.4 Output Stage

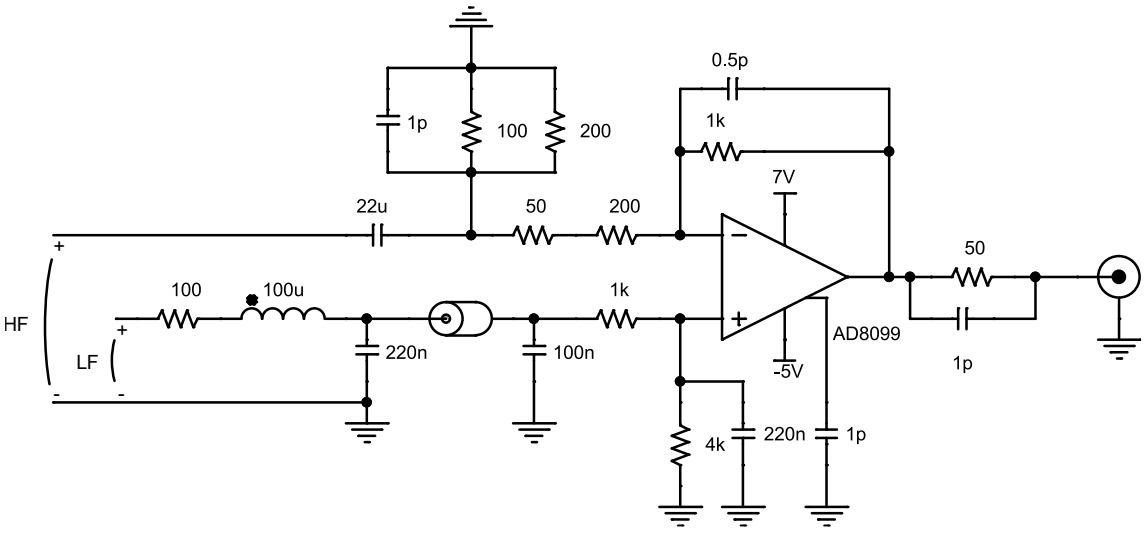

Figure 16 – Simplified schematic of the output stage.

The output stage joins the high and low frequency paths. The amplifier implements summation by connecting each path to its own input. In respect to the high frequency path, the amplifier is an AC coupled negative feedback amplifier. In respect to the low frequency path, it is a DC coupled positive feedback amplifier. The frequency response of each path is overlapping, and a digital filter is used to smooth the transition.

The low frequency path is output from the DAC and then filtered locally to remove quantization effects. At the positive input of the output amplifier, a ferrite and capacitor form a low pass filter to remove noise coupled onto the short transmission line connecting DAC and amplifier. It also serves as an additional quantization filter, although this is a secondary effect.

The high frequency signal is taken at the input to the PLL VCO. If the loop is locked, the impedance looking into the node is 0Ω, as the control loop rejects changes. Thus, it can be treated as an ideal voltage source. A series resistance will then provide impedance matching between the source and the output buffer amplifier. The amplifier itself is matched by the impedance network at the amplifier's negative input.

3.2.5 Estimation of Parasitic Impedances

The parasitic elements are estimated through Equation 50, using the actual footprint, with a dielectric height of 0.18 mm, copper thickness 35 µm and with a relative permittivity of 4.2. Dimensions related to the PCB stack-up are obtained from the PCB manufacturer. The result is summarized in Table 3.

Table 3 – Estimation of parasitic impedances.

	Inductance	**Capacitance**	**w/h**
0402 pad	0.08 nH	0.11 pF	3.37
0603 pad	0.05 nH	0.58 pF	5.62
50Ω TL	0.26 nH/mm	0.11 pF/mm	1.80

As Equation 50 is only valid for moderate w/h, here assumed to satisfy w/h < 3, the validity of the 0603 package parasitics is suspect. As no 0603 packages are used at sensitive nodes, the impact of the error should be negligible.

3.3 Supporting Circuitry

3.3.1 Laser Bias Current

ADN2830 from Analog Devices is used to generate the bias current the laser requires. It has an integrated control loop which forces the bias current to adjust to changes in optical output power. The laser has an integrated monitoring photodiode which serves as a reference.

The output current stage expects the laser diode cathode to be tied to supply voltage. The chosen laser, however, has its cathode internally tied to ground. This issue may be solved by tying the output to a PMOS current mirror and connecting its output to the laser. Because this is wasteful in terms of energy, it is not an ideal solution. Nevertheless, it was used in the prototype due to an oversight.

3.3.2 Battery Management

The sensor head is powered by a lithium battery, Panasonic PA-L46.K03.R001, with 16.2 Wh capacity. A worst-case power consumption analysis gives a minimum operating time of 4.5 h. Recharging of the battery is handled by LTC4061 from Linear Technology. It has the necessary safety functions such as total charging duration, maximum/minimum charge current as well as temperature monitoring.

3.3.3 Power Supplies

The same type of power supplies is used in both sensor head and receiver. A switched converter, Linear Technology LT3999, followed by a linear converter, Linear Technology LT3045 for positive voltages and Analog Devices ADP7182 for negative voltages.

The switched converter is of push pull type and its switching voltage is applied over the primary windings of a transformer, TDK B82805A0 series, which gives an unregulated voltage over the secondary windings. The voltage is rectified by Schottky diodes, Rohm RB550EAFH. It also has duty cycle control which means that the output voltage remains steady, for a given load, over a given input voltage range. This is preferable in the sensor head, where the battery voltage will vary with charge and setting a fixed, higher, voltage would result in losses. While a converter with line control could have been used, the ones considered required more surrounding circuitry. In hindsight, converters with line control would have been preferable as their output voltage would have been more reliable.

In the receiver, conversion from 230 V to 5 V is performed by an AC/DC converter (Recom RAC10-05SK/277), before being applied to the low voltage switched converters.

3.3.4 Temperature Control

As an alternative to the low frequency path, temperature control of the VCO is also added to the prototype. The VCO temperature is sampled at the sensor head and sent to the receiver, where it acts as reference to a heating element placed as close as possible to the PLL reference VCO. If it is possible to maintain both VCO's at the same temperature, the low frequency signal chain may be eliminated. This is assuming that the VCO is the major source of temperature drift related errors.

3.3.5 Alternate Power Sources

As an alternative to powering the sensor head with a battery, power may be transmitted by optical fibers. Such solutions are quite expensive however, and highly specialized. Only two manufacturers have been found even after extensive searching. Quotations have been obtained for a system that can deliver up to 0.5 W of electrical power and are listed in Table 4.

Table 4 – Quotations of devices for optical power transmission.

Manufacturer	**Distributor**	**Product(s)**	**Cost**
MH GoPower	MH GoPower	PPM-0002 together with YCH-L240 PPC	$500*
Lumentum	Laser 2000	PPM-500-K-FC-6E-200	$1880

*Discounted price.

As the devices lack the necessary output power for the system as is, it will be necessary to either decrease the sensor head's power consumption or to use devices with higher output power. It has not been ascertained if Lumentum offer higher power devices, but MH GoPower does. Their assortment includes devices with an output power up to 10 W.

While optically transmitted power is appealing for long term measurements, safety issues may limit the environments in which it can be used. It is, however, possible to comply with safety regulations if faults can be detected and the laser be shut off sufficiently fast. Even so, the obvious safety concern is why a battery powered solution is chosen for the prototype.

Chapter 4

The Prototype

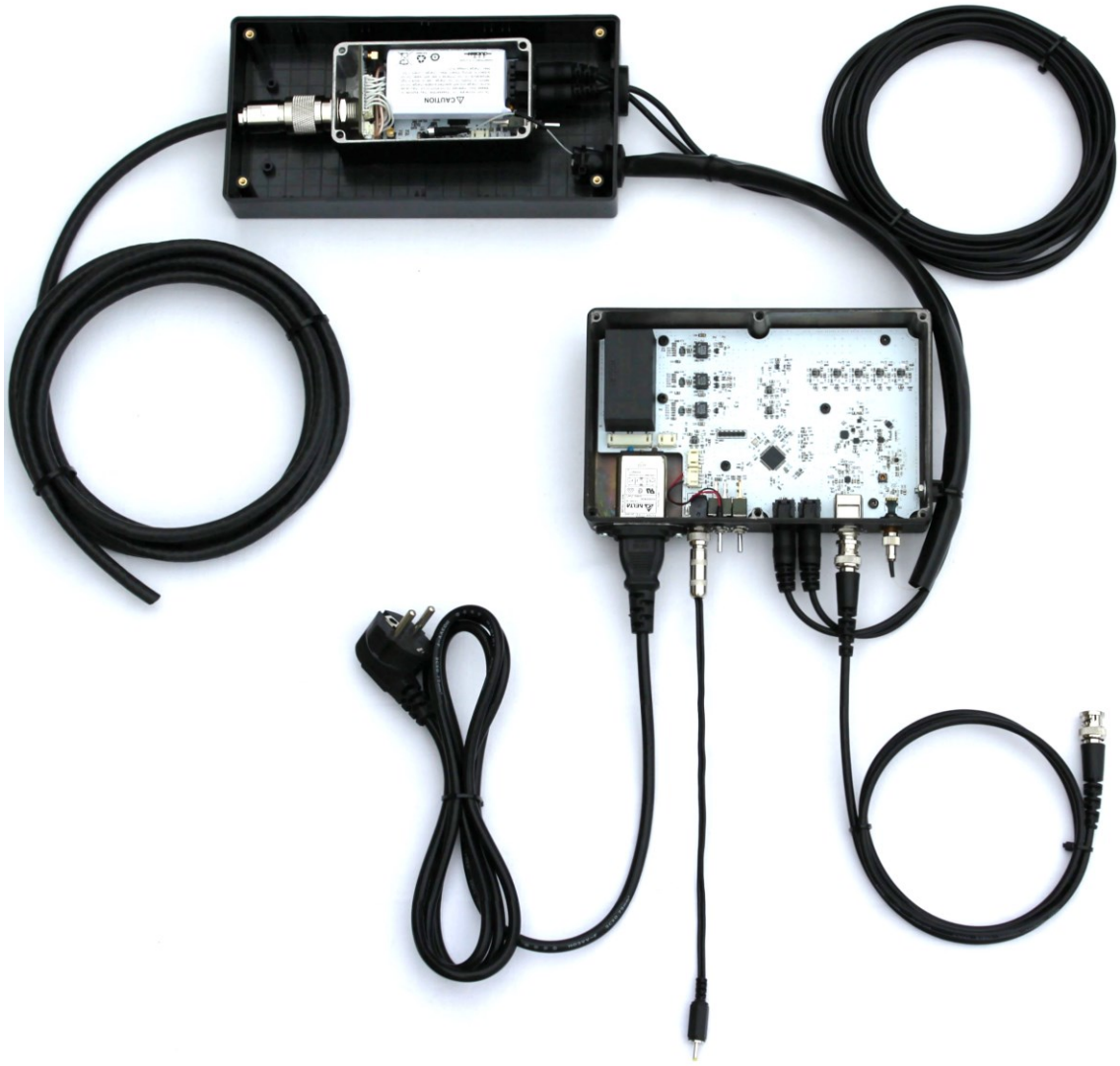

Figure 17 – The prototype.

Figure 17 shows the assembled prototype. The sensor head and receiver are interconnected by three optical fibers and a cable used for charging the sensor head's battery. One of the fibers is a single mode fiber, carrying the high frequency path. The other two are plastic fibers with TOSLINK connectors. During an active measurement, only the fibers are connected. Connecting the charging cable during an active measurement would result in

catastrophic levels of current. To avoid such an inconvenient scenario, the charging cable is made short such that the sensor head has to be physically removed from the measurement object before being charged.

At the receiver side, there are additional connections to line power and to external measurement equipment through a BNC connector. Furthermore, there are switches on the front for power/sensor head standby and DC calibration. Figure 18 shows these connectors and switches.

Figure 18 – Receiver as seen from the front.

At the sensor head, a shielded twin axial cable is connected to the measurement object in the fashion described in Section 3.1. Since the shield is connected to the sensor head enclosure, the enclosure is at the measurement potential. Thus, it needs to be electrically isolated and it is made so by enclosing it within a plastic box. The size of the box can be reduced significantly if tailored to the dimensions of the metallic enclosure but for a prototype, the larger box shown in Figure 19 is sufficient.

Figure 19 – Sensor head mounted in a plastic enclosure.

The sensor head consists of two separate boards, one containing the input stage and VCO (furthest to the right in Figure 19), the other the laser as well as supporting circuitry such

as power converters, MCU and ADC (beneath the battery in Figure 19). They can be seen in Figure 20 and Figure 21 respectively. The reason for separating the two is mostly due to space constraints, where the size of the battery and coaxial connector are the limiting factors.

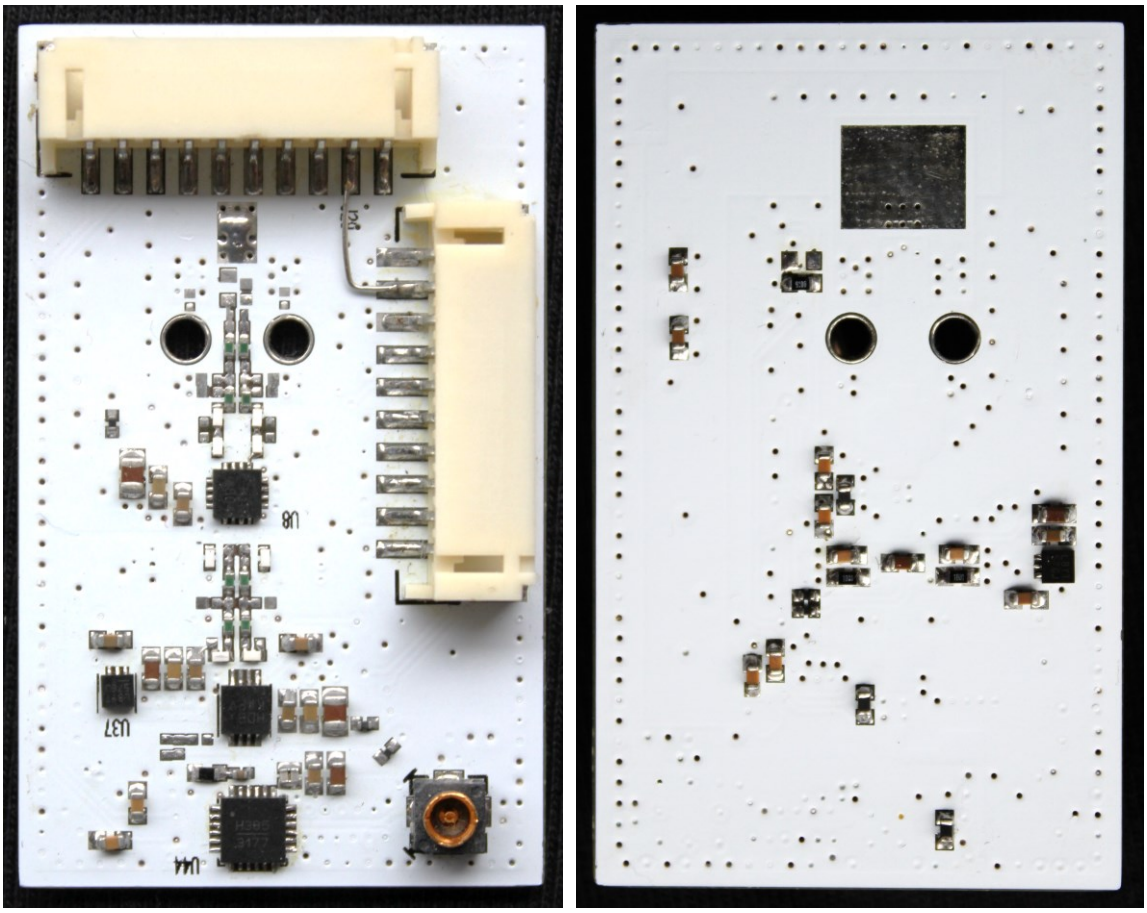

Figure 20 – The sensor head input stage. Top side is seen in to the left and the bottom side to the right.

The components seen on the board topside in Figure 20 are, from top to bottom, differential amplifier, single ended amplifier, VCO. The high frequency path is output through the MMCX connector, in the lower right, and the low frequency path is output through the right-side 10-pole connector. The two through holes is for the, yet unconnected, twinaxial connector.

The second board in the sensor can be seen in Figure 21. The topside is shown in the leftmost picture. To the right of the center is the analog laser. The IC controlling its bias current, can be seen centered in the lower part of the board. In the center, the MCU is placed along with common mode filters for measurement of the low frequency path as well as various temperatures. The five ICs along the left side are all linear power converters. At the bottom side of the board, seen in the right most picture, two switched power converters are seen. These are placed at the bottom-side of the board to provide maximum

separation to the sensitive topside circuitry. In the top left corner is the battery charging IC.

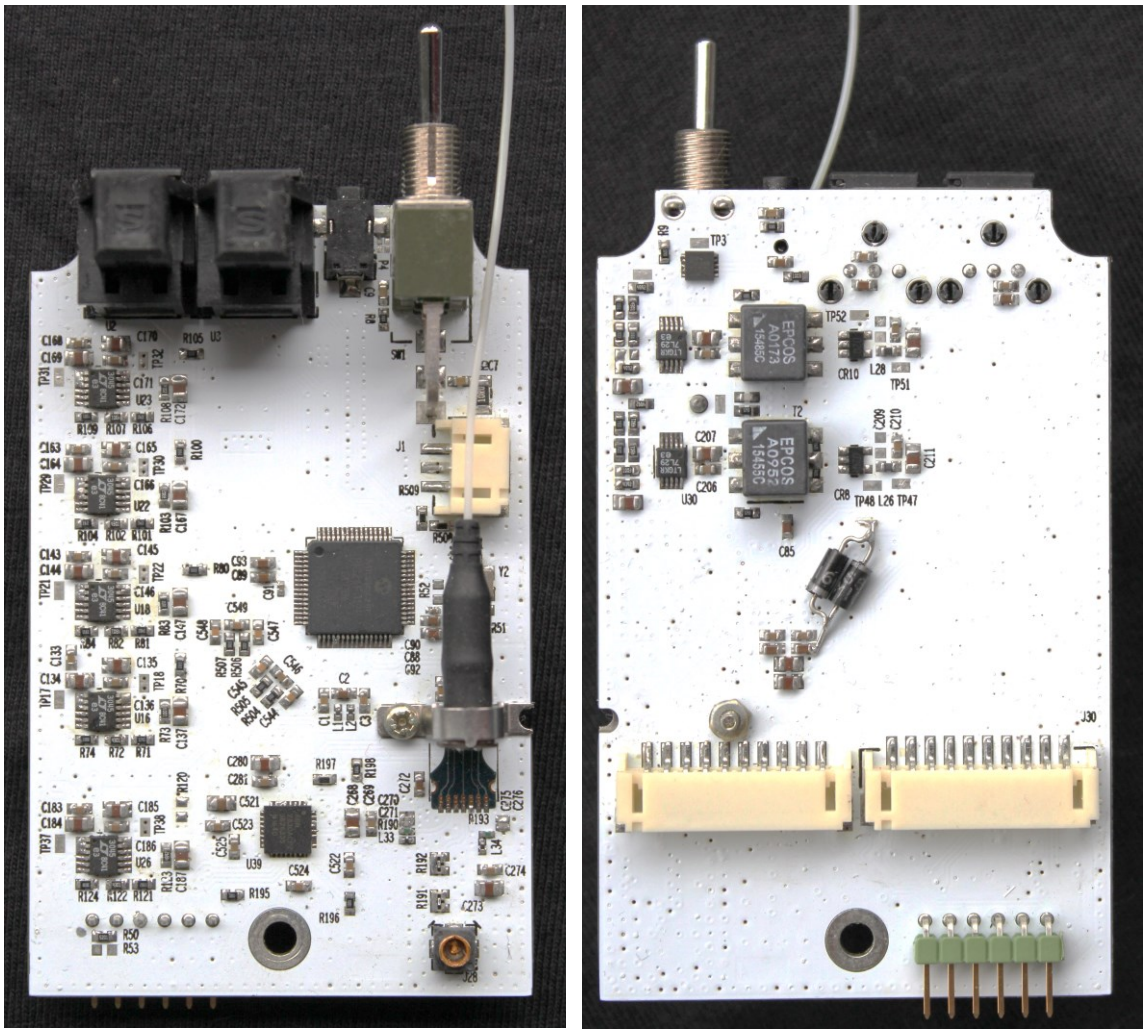

Figure 21 – Second board in the sensor head. Top side is seen in to the left and the bottom side to the right.

The two paralleled diodes constitute a fix to make sure analog and digital power are always within one diode drop of each other. The two rails are supplied from different switched converters which means the rails have different ramp times. The MCU have similar internal diodes and the external ones make sure damage is not inflicted during the rails' ramp-up or during a fault scenario. Ideally, the rails should have been supplied from the same linear converter and instead separated by passive filtering.

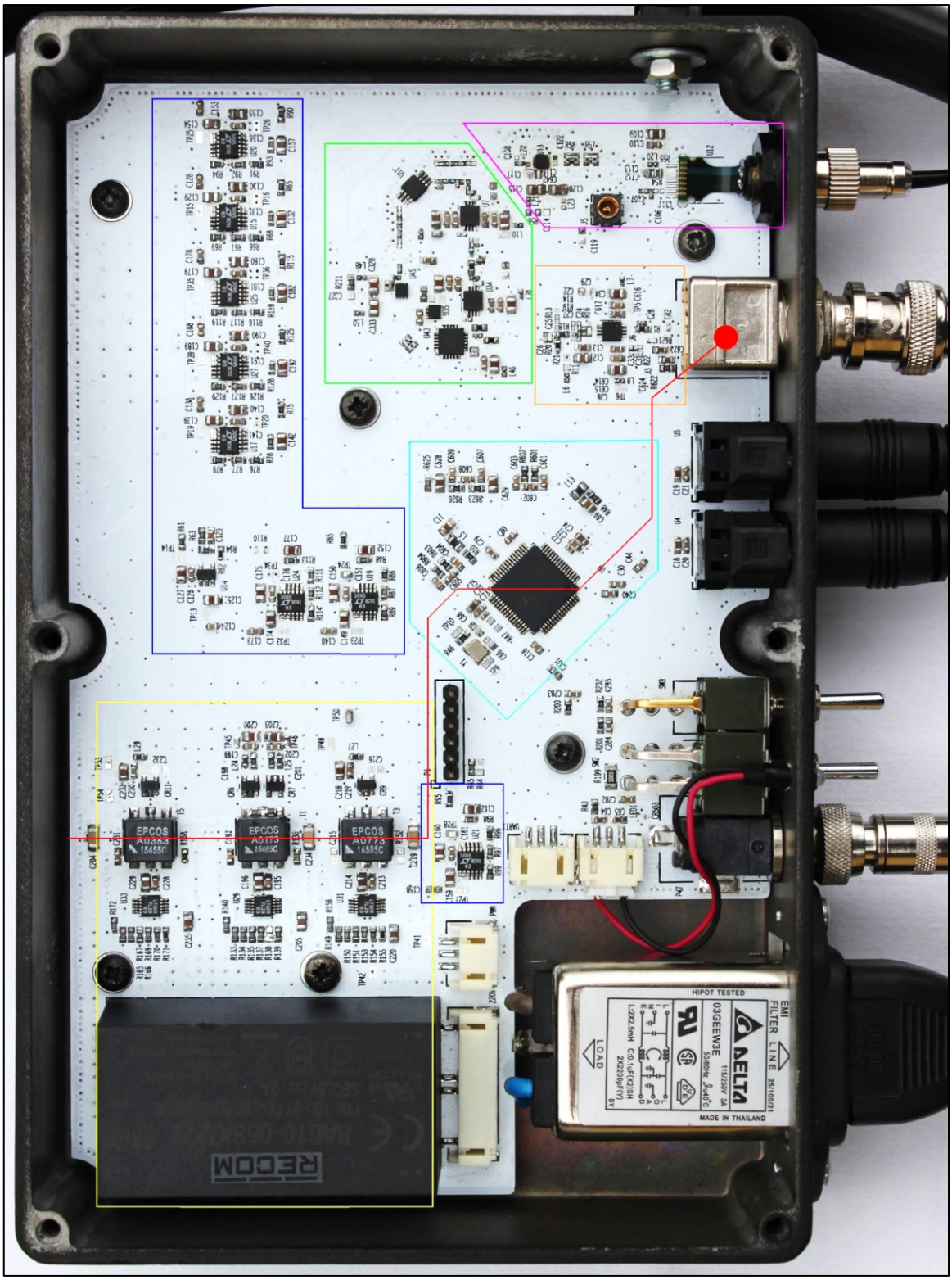

Figure 22 – Receiver.

The receiver can be seen in Figure 22. The switching power converters (3+1) are located in the lower left, encompassed by the yellow rectangle. These converters share ground with the digital ground plane which is split from the analog beneath the red line. Capacitors located at the switched converters shorts the two ground planes at higher frequencies to provide a local return path for currents mainly stemming from transformer interwinding capacitance. Both ground planes are shorted by the output BNC connector (red dot in Figure 22). The MCU has both analog and digital ground references and these are tied to their respective ground planes. The DC resistance is ~3 Ω between the two MCU ground pins so DC current between the planes is expected to take the path through the short rather than through the ground pins. There is no intended current between the two planes, apart from enable signals carrying small DC currents. Digital switching noise imposed on the enable signals is local to their traces, as they are routed over the ground plane. The possible sources for current injection between the two planes are the switched converters, where their shorting capacitors makes their current local, and the MCU, which is assumed to have an internal low impedance connection at its operating frequency. Thus, there should be no large current loops between planes.

The PLL is within the confines of the green line, the output stage, within the orange, the MCU within the light blue and the photo detector, and input limiting amplifier, is within the pink line. Encircled by the blue lines are the linear power converters. Their placement ensures that current drawn by the converters are steered away from the analog circuitry to the largest extent possible.

There is one layer dedicated as a reference plane and it is split beneath the red line as mentioned earlier. This reference plane is used both for signals and power. Since the frequency of the power supply current drawn is on the order of tens of kHz, due to individual decoupling, it can be a problem in respect to the DAC, outputting the low frequency path. However, its signal level is large and can allow for around a mV of ground interference without impacting the output SNR. In respect to the PLL, its control loop configuration rejects low frequency noise very well. It is assumed that this applies to all noise, even correlated noise from the supply current drawn from the devices within the loop. The conclusion is then that ground plane noise is not expected to be problematic in terms of dynamic range.

In the terms of spurious free dynamic range, however, the single ended amplifiers might be limiting factors at the end of the passband. With only one reference plane, the negative power pin is tied in close proximity to the input filter ground by necessity. This means that a part of the supply current is fed back to the input, causing distortion.

It is difficult to mitigate this interaction with a shared reference plane. Attempts have been made by inserting splits in the ground plane where space permitted, but in most cases doing so was not possible. All metal is also removed directly beneath the amplifier inputs for stability reasons. It has the added benefit of also decreasing coupling between supply pins and input pins. A 6-layer stack-up would have greatly improved the layout by allowing separate reference planes for power and signal.

The reference plane is joined with the enclosure at essentially each external connection (switches, line filter, BNC). One of the cases where this is expected to be meaningful is in reducing unintended interaction between external measurement equipment and receiver. A short is made between the coaxial cable shield and protective earth through the line filter, which has its protective earth input tied to the enclosure.

Chapter 5

Results and Discussion

Results are obtained through SPICE simulations in ADIsimPE. The entire signal chain is simulated apart from the optical link between modulating VCO and PLL input. The link is assumed to have a transfer function with constant gain and phase. The gain is accounted for by setting a fixed input power to the PLL.

Parasitic impedances are accounted for at relevant nodes and are estimated by considering the component pads as microstrips, with length equal the length of the pad. Since all components are placed with the shortest possible spacing, the interconnection line length is, in most instances, assumed to be zero. In addition, and more importantly, s-parameter models are used for all passive components. These are obtained from the manufacturer, in most instances Murata which supplies models for all their passive components.

The transfer function from each simulation is processed in MATLAB to arrive at a desired digital transfer function that joins both the high frequency path and the low frequency path with minimum disturbance.

In order to validate the proposed concept, a prototype is designed and built. However, due to insufficient time, it has not been properly debugged to obtain meaningful measurements. In light of this, in this section, the prototype is only mentioned in respect to its current status.

5.1 The Phase Locked Loop

The model used to simulate the frequency response of the PLL can be seen in Figure 26. “Measurement 1” is taken from the input to the modulating VCO, to the input of the reference VCO. It corresponds to the transfer function from input stage to output stage and is denoted the PLL full transfer function. Its response can be seen in Figure 23. “Measurement 2” is the transfer function of the loop filter.

Figure 23 shows the PLL transfer function for different loop filters. Three types of loop filters are considered, and their characteristics can be seen in Figure 24. “high gain” and “low gain” corresponds to amplifiers with fixed gain and “integrating, with both amplifiers in open loop, with only parasitic impedances between the individual amplifier’s input and output. “integrating” corresponds to the exact setup given in Figure 26. In Figure 26, low cost general-purpose resistors are used in all cases, except for the IF port match, and they are approximated by RLC type circuits. For the fixed gain simulations, s-parameterized RF resistors are used.

In Figure 23, it is seen that “high gain” and “integrating” have similar amplitude deviation in the passband, but “integrating” has worse phase characteristic. “low gain” clearly has a worse amplitude response in the passband, but similar maximum phase deviation in the passband. It is also considerably closer to instability than the other two.

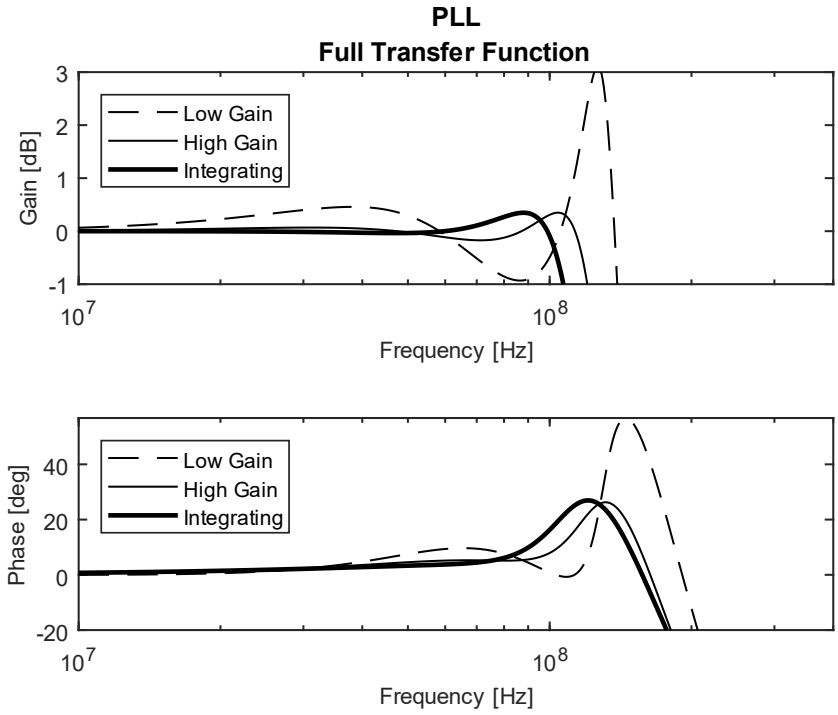

Figure 23 – The PLL full transfer function as defined by "Measurement 1" in Figure 26.

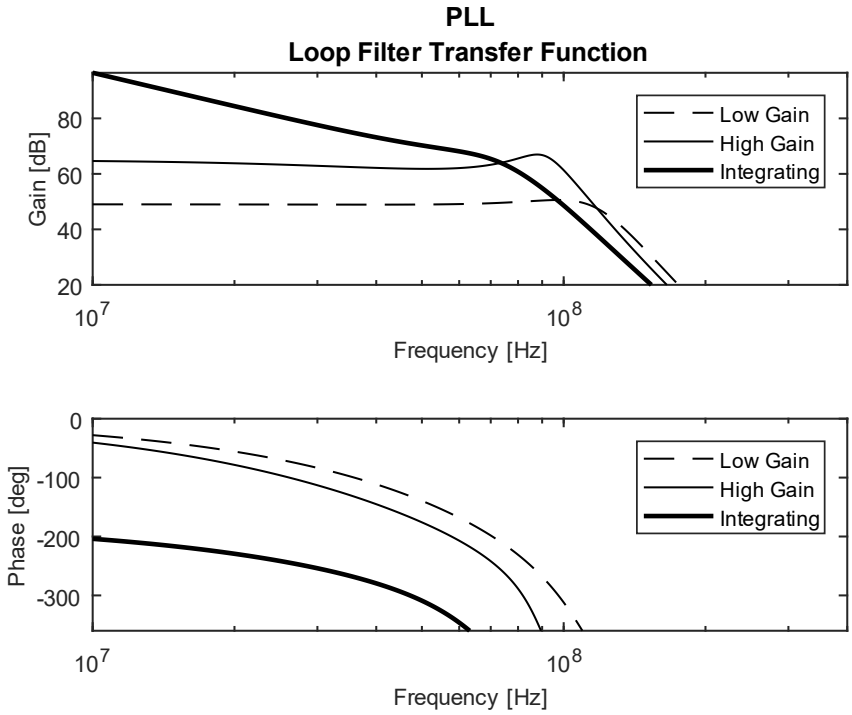

Figure 24 – The loop filter gain as defined by "Measurement 2" in Figure 26.

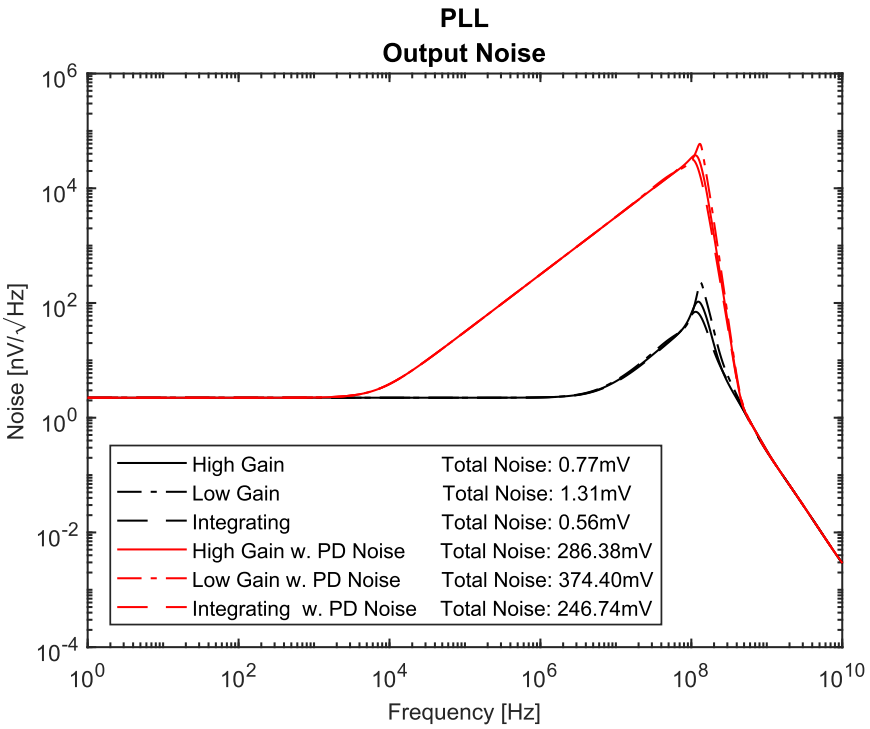

Figure 25 – The output noise as defined by "VOUT" node in Figure 27.

It is of interest to compare how the two gain settings affect the output noise. Figure 27 shows the simulation setup used to determine noise. It is similar to Figure 26 apart from the s-parametrized resistors which are replaced with ideal ones to simulate thermal noise. The output noise for the various gains, with or without a noiseless phase detector, is given in Figure 25. To simulate the phase detector noise, a resistor, as given by Equation 68, is inserted at the phase detector output to simulate noise generated by the mixing of amplitude noise at the RF port, with the signal at the LO port. The amplitude noise corresponds to an RF port that is tied directly to the photo detector output i.e. without an amplitude limiter. It is obvious from Figure 25 that the noise at the photo detector output is far too high to be able to use its output without amplitude limiting amplifiers to reject amplitude noise.

As for the noise dependency, the different filters produce similar output noise. The difference is due to their different bandwidths, which is in accordance with Figure 5. Thus, considering the decreased cost of having the amplifiers in open loop, as no expensive RF resistors need to be used, the open loop "integrating" loop filter is used in the PLL.

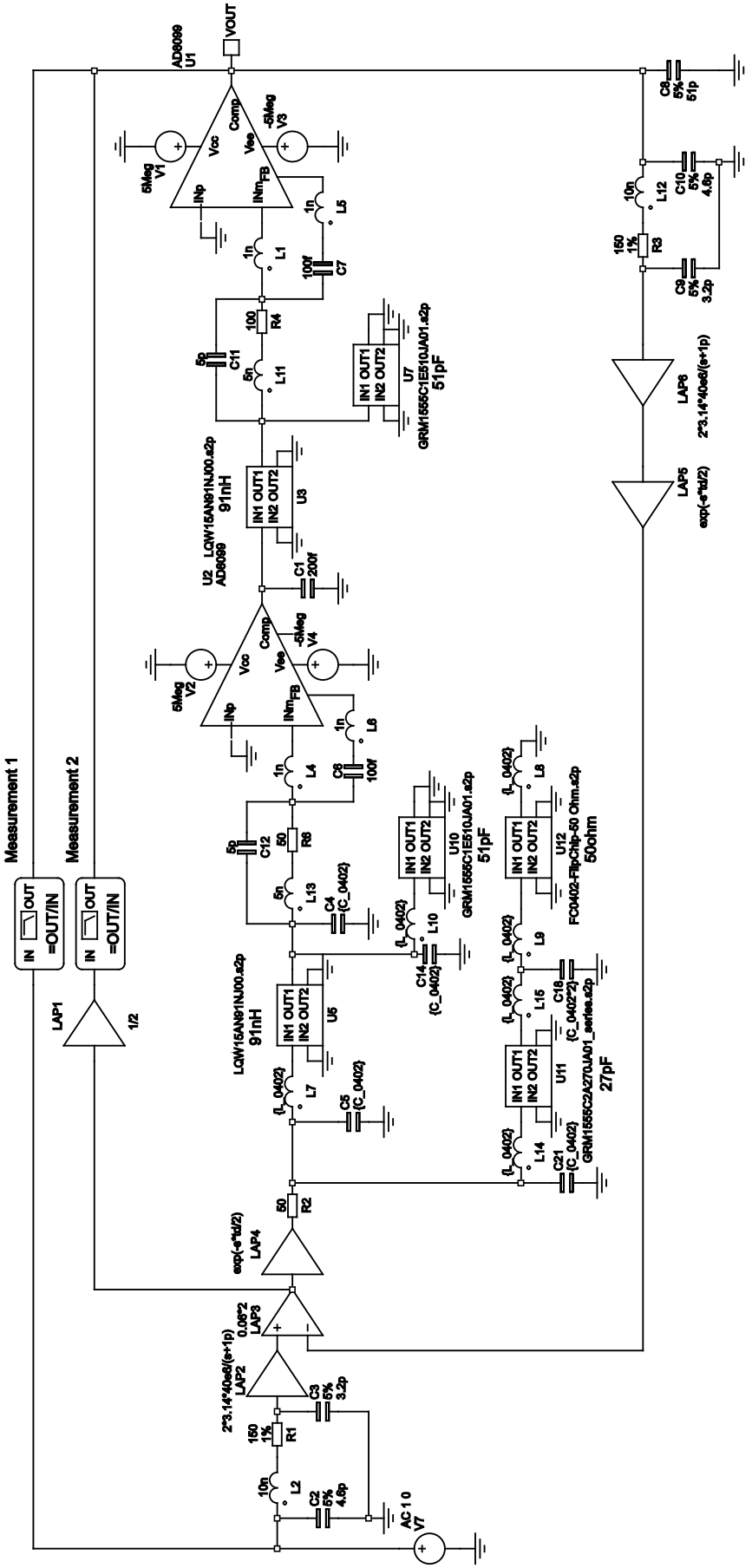

Figure 26 – PLL simulation model setup in ADIsimPE.

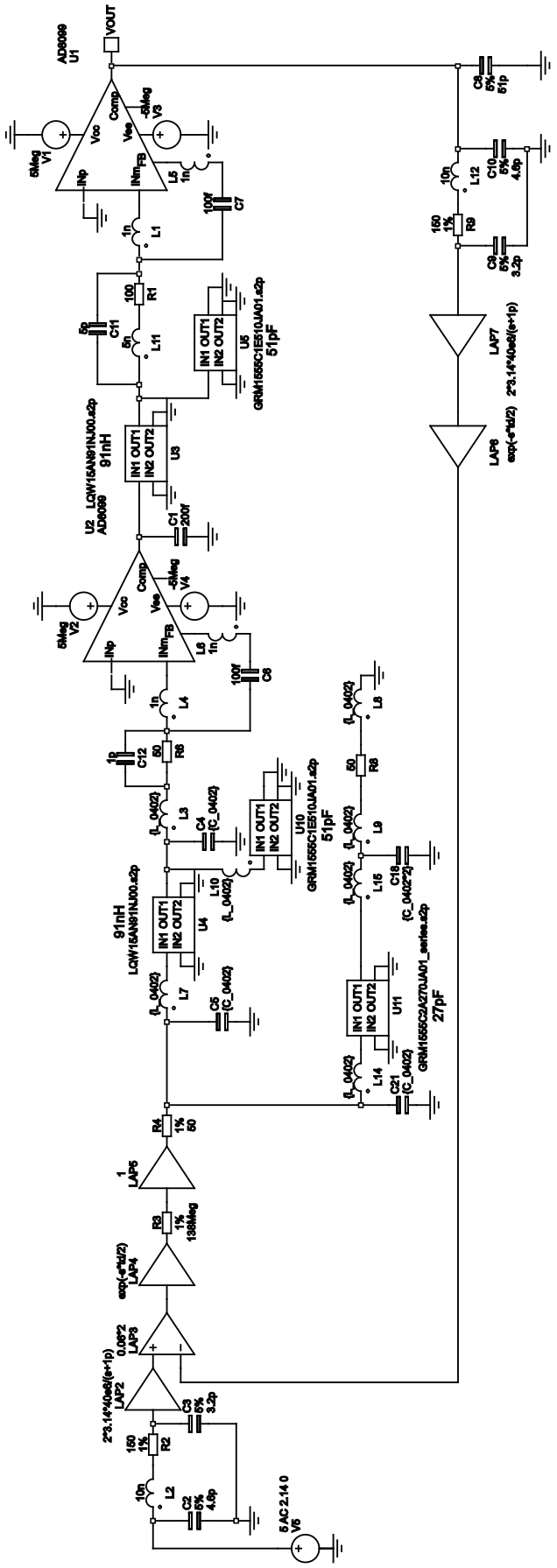

Figure 27 – PLL noise model setup in ADIsimPE.

5.2 Input Stage

The input stage amplifies the measured signal and splits it into a high- and low frequency path. For details on the circuit, see Section 0. The input stage simulation model can be seen in Figure 30 and is in direct correspondence to the simplified schematic given in Figure 15. The high frequency path is defined by "Measurement 1" and the low frequency path by "Measurement 2", as given in Figure 30. The latter has its output referenced at the ADC input, hence the double common mode filters seen to the lower right in Figure 30.

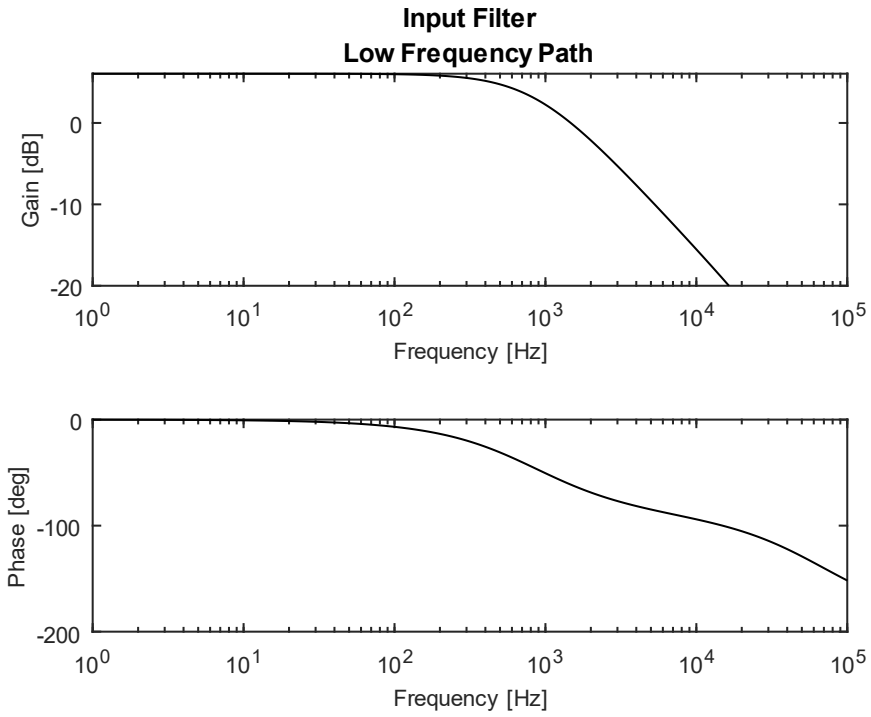

Figure 28 – Low frequency response of the input stage as defined by "Measurement 2" in Figure 30.

Figure 28 shows the low frequency response. It has a differential passband gain of 6 dB with a -3 dB corner frequency at 900 Hz. Since the signal level is quite low, 60 mV peak, the ADC that samples this signal has a (integrated) differential input amplifier which further amplifies the signal before digitization. This gain is assumed to be part of the digital transfer function, which has yet to be determined.

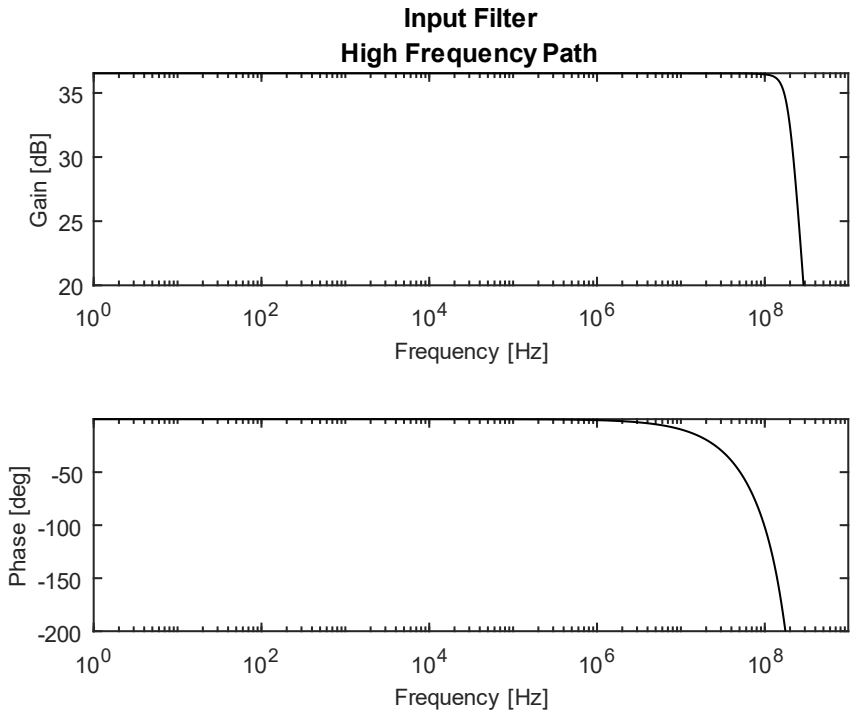

Figure 29 – High frequency response of the input stage as defined by "Measurement 1" in Figure 30.

The high frequency response is shown in Figure 29 and shows a flat amplitude response with a -3 dB corner frequency at 190 MHz.

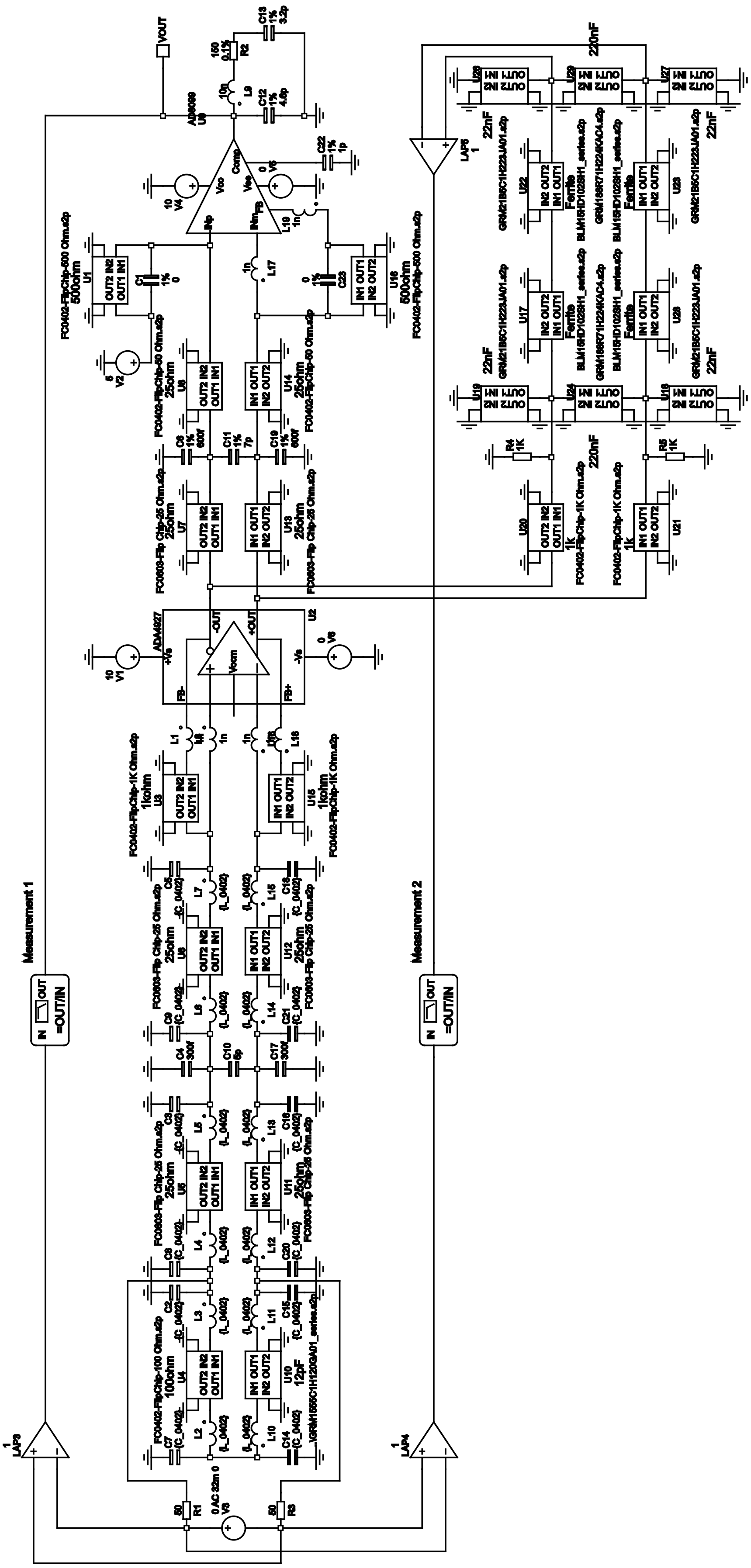

Figure 30 – Input filter simulation model setup in ADIsimPE.

5.3 Output Stage

The output filter joins the high- and low frequency paths. For details, see Section 0. The simulation model is shown in Figure 32 and corresponds to the simplified schematic given in Figure 16. The DAC source impedance is assumed to be zero, and the PLL output impedance is set 50 Ω. The output is referenced at the external measurement equipment and is assumed matched to 50 Ω. Since the amplifier SPICE model does not correctly account for output impedance, its output is tied to an ideal buffer amplifier. It is assumed that a perfect matching can be obtained in the actual design and this matching constitutes the two output resistors.

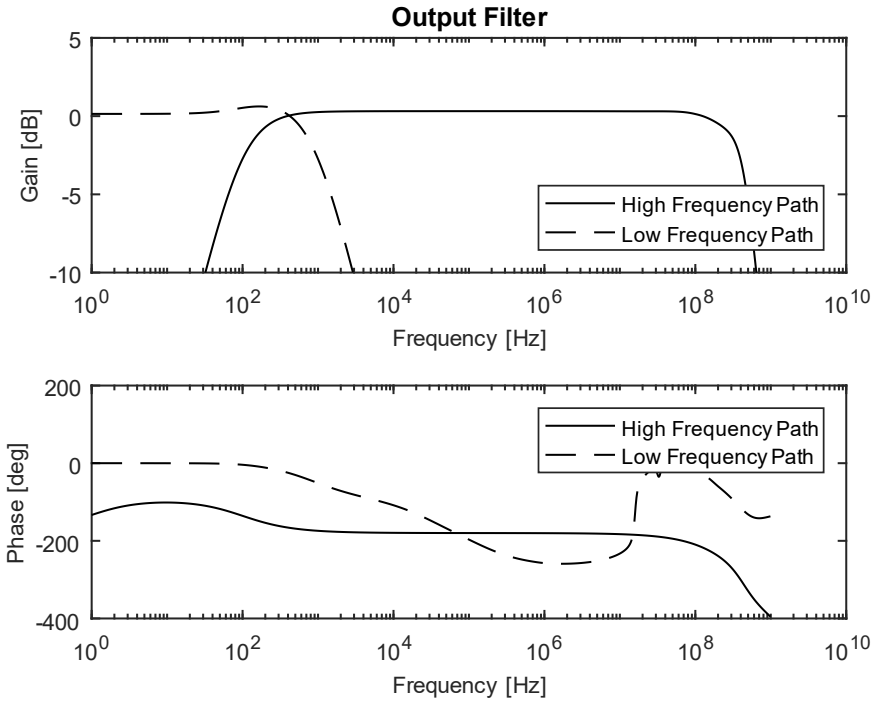

Figure 31 – Output filter response to the low and high frequency paths plotted separately. The low and high frequency path is defined by "Measurement 1" and "Measurement 2" respectively in Figure 32 .

From Figure 31 it is seen that the high- and low frequency paths have an overlapping response between 100 Hz and 1 kHz. A digital filter is used to smooth the transition.

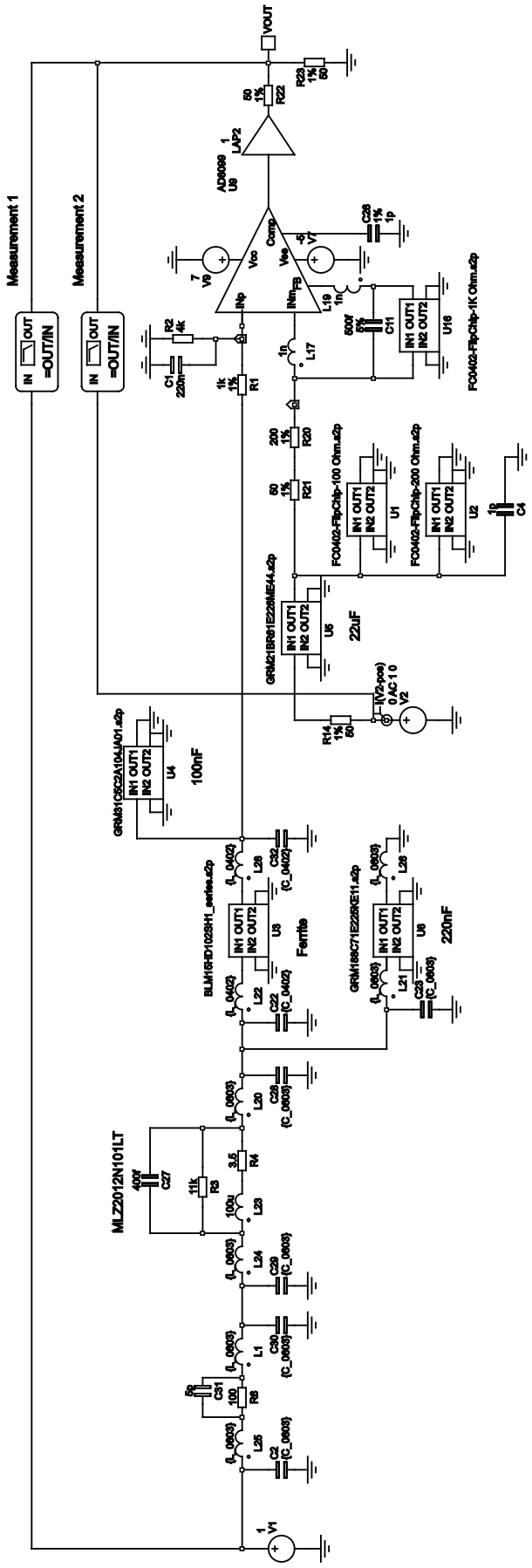

Figure 32 – Output filter simulation model setup in ADIsimPE.

5.4 Combined Result

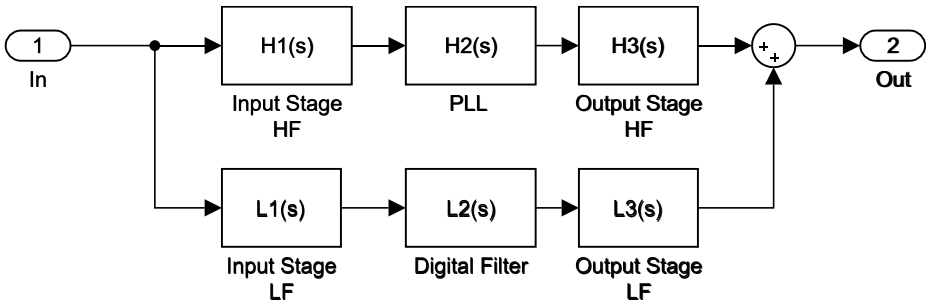

Figure 33 – Block diagram of the relation between the different simulated responses.

The simulation results obtained thus far are measured at nodes such that they can be represented, and interconnected, by ideal transfer functions. The full system can be seen in Figure 33, where the correspondence between individual transfer functions and the previous figures is given in Table 5.

Table 5 – Correspondence between transfer functions defined in Figure 33 and previous figures.

	Figure	**Notes**
H_1	Figure 29	
H_2	Figure 23	
H_3	Figure 31	"High Frequency Path"
L_1	Figure 28	
L_3	Figure 31	"Low Frequency Path"

The desired digital filter function can then be obtained by rewriting the total transfer function defined by Figure 33.

$$G = H_1H_2H_3 + L_1L_2L_3 \Leftrightarrow L_2 = \frac{G - H_1H_2H_3}{L_1L_3} \tag{70}$$

Since the desired amplitude response of the full transfer function, G, is constant, G can be replaced by a constant equal the gain of the high frequency path in its passband i.e.

$$L_2(j\omega) = \frac{H_1(j\omega_1)H_2(j\omega_1)H_3(j\omega_1) - H_1(j\omega)H_2(j\omega)H_3(j\omega)}{L_1(j\omega)L_3(j\omega)} \tag{71}$$

Where ω_1 is in the flat region of the high frequency response. The system can be simplified by curve fitting $L_2(j\omega)$ over a smaller frequency range. Using the MATLAB function "tfest", $L_2(j\omega)$ is data fitted over the frequency range 1 Hz – 10 kHz to yield the following approximation.

$$L_2(s) = \frac{-1.202 \cdot 10^{-6} s^4 - 8164 \cdot 10^{-3}\, s^3 + 38.92\, s^2 + 5.808 \cdot 10^4\, s + 2.468 \cdot 10^7}{s^2 - 7884\, s - 7.244 \cdot 10^5} \quad (72)$$

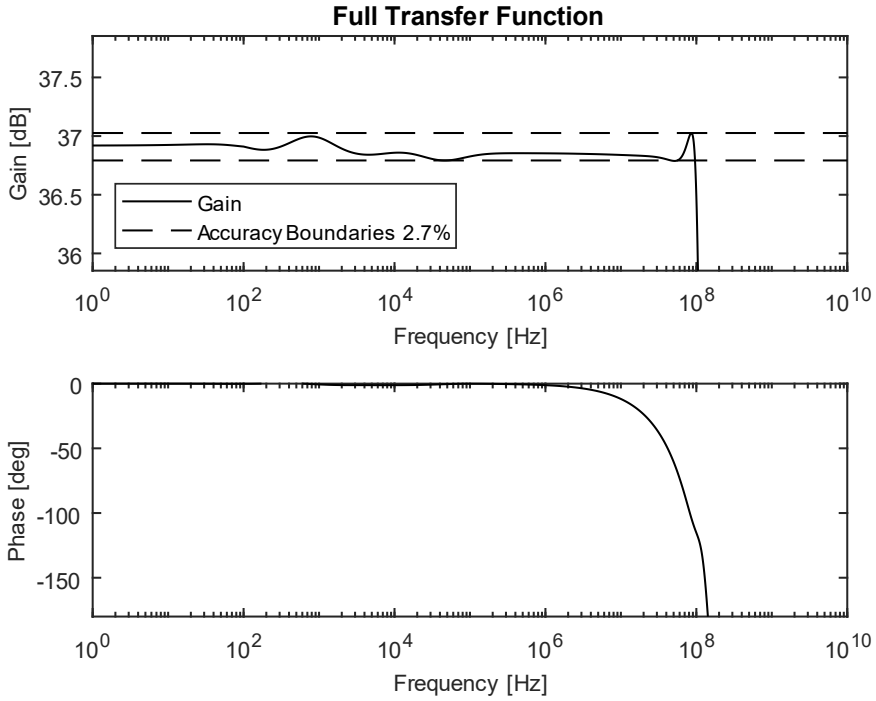

Figure 34 – Full transfer function, from measurement node to system output.

The total transfer function, G, is given in Figure 34. It shows a passband accuracy of 2.7 % and a phase shift of 64° at 100 MHz. Since the amplifiers are slewrate limited, the output voltage is limited to 2.14 V. By dividing by the gain, a sinusoidal input is limited to 21.4 mV RMS. This may be increased up to 35 mV RMS for lower frequencies, but larger values will saturate amplifiers.

The output noise can be analyzed in a similar fashion by adding the separate noise simulations at the output amplifier. The individual noise sources are given by the VOUT node in Figure 27, Figure 30 and Figure 32. In all instances, resistor s-parameter models are replaced by ideal resistors. The output noise is then

$$N_v = \sqrt{N_{PLL}^2 |H_3(s)|^2 + N_{IN}^2 |H_2(s)|^2 |H_3(s)|^2 + N_{OUT}^2} \quad (73)$$

Where N_{PLL}, N_{IN} and N_{OUT} is the voltage noise associated with the PLL, input amplifier and output amplifier respectively.

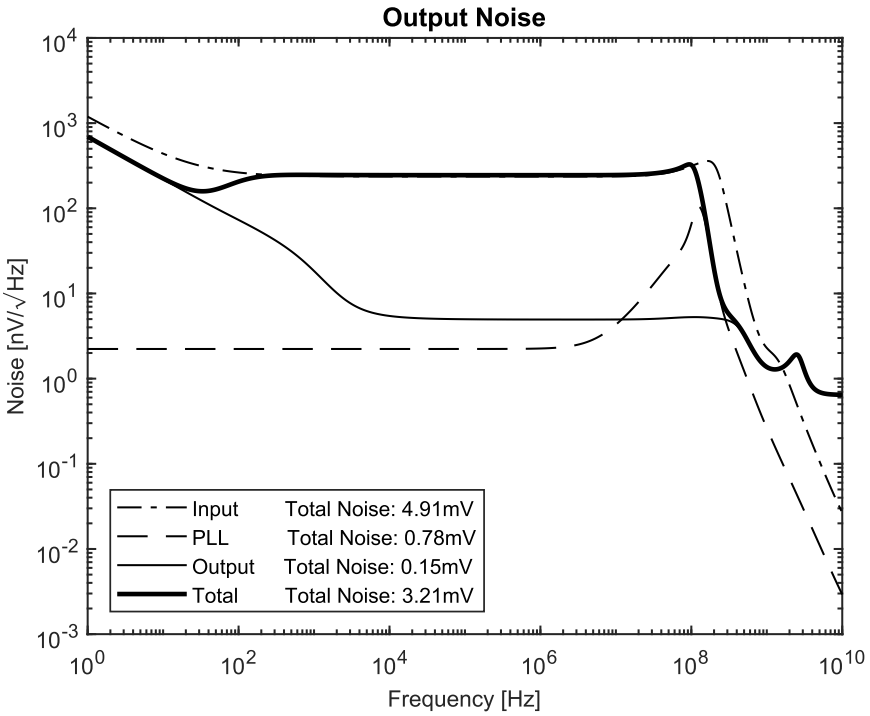

Figure 35 – Output noise of the full system.

The noise is plotted in Figure 35. It is seen that noise associated with the input stage is considerably higher than other noise sources. This is due to the high amplification necessary to amplify the small input signal. If larger input signals are allowed, the noise may be decreased to similar levels as the output stage. This corresponds to a decrease in voltage noise by 6 times or, equivalently, a 16 dB dynamic range improvement. In practice, the output noise will likely depend on how effective the amplitude limiters are in limiting noise.

Having obtained the output noise, the dynamic range can also be evaluated. So far, noise contributed by the FM transmission itself has not been considered. The dynamic range of the FM transmission is described by Equation 12 and the noise can be calculated by knowledge of the modulating voltage. Since this noise is uncorrelated with the noise in the amplifier chains, seen in Figure 35, they may be added RMS wise. Rewriting noise into dynamic range gives

$$N^2 = N_1^2 + N_2^2 = \left[S = \frac{P}{N} = R_{DR}^2 \Rightarrow N = \frac{P}{R_{DR}^2}\right] \Rightarrow \frac{P^2}{R_{DR}^4} = \frac{P^2}{{R_{DR_1}}^4} + \frac{P^2}{{R_{DR_2}}^4}$$

$$\Leftrightarrow R_{DR} = \frac{1}{\left(\frac{1}{{R_{DR_1}}^4} + \frac{1}{{R_{DR_2}}^4}\right)^{\frac{1}{4}}} =$$

$$= \frac{1}{\left(\frac{1}{\left(21.4[mV]\frac{|G(jf)|}{\sqrt{\int_B N_V^2 df}}\right)^4} + \frac{1}{S\left[\frac{21.4 \cdot \sqrt{2}[mV] \cdot |H_1(jf)|K_{VCO}}{f}\right]^2}\right)^{\frac{1}{4}}} \quad (74)$$

Where the two terms are given by the maximum signal voltage over the integrated noise floor (Equation 73) and, the square root of the SNR due to the FM transmission itself as given by Equation 12. The CNR used in Equation 12 was previously calculated to 34.2 dB. The input voltage to the VCO, described in Equation 12, is multiplied with the appropriate transfer function to give the correct frequency dependency. Note that the way dynamic range is defined, the dynamic range is given in the time domain i.e. it is the square root of the signal to noise ratio at maximum signal amplitude. Furthermore, the way modulation index is used, it is also only strictly valid for single sinusoidal inputs.

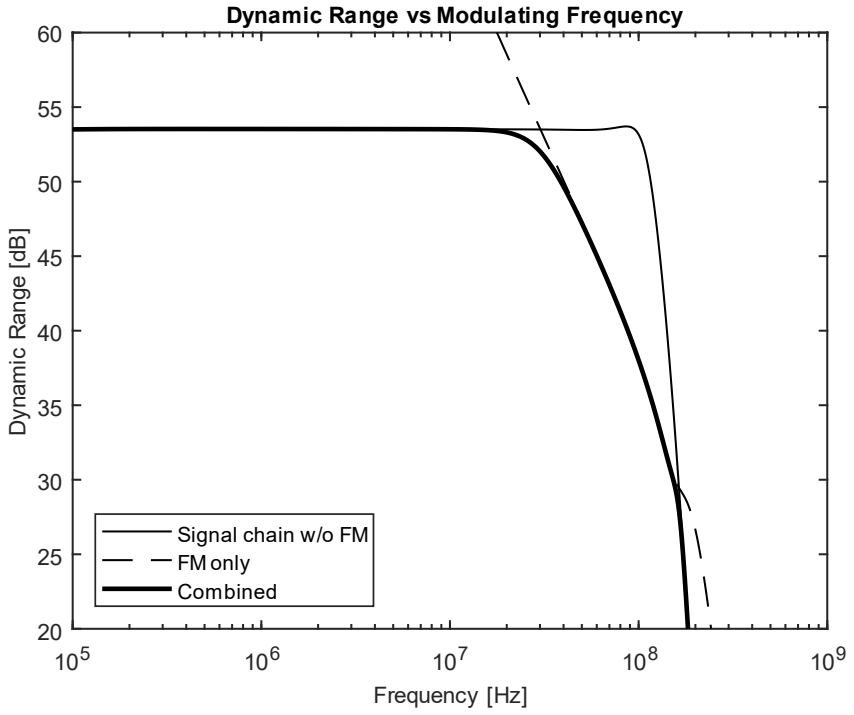

Figure 36 – Dynamic Range of the full system.

Equation 74 is plotted in Figure 36 and shows a dynamic range of 53 dB for frequencies less than ~20 MHz, and 38 dB at the passband end at 100 MHz. Again, note that the DR is ultimately limited by the low amplitude of the measured signal. A dynamic range improvement of up to 16 dB may be achieved by increasing it.

By considering the modulation index, it is seen that the dynamic range at the end of the passband can be increased by increasing the amplitude at the VCO or by choosing a VCO with higher gain. The former is possible only if amplifiers with higher slewrate are chosen. Out of the considered VCOs, the ones which had high gain only had so over a small voltage range. Since this is obviously conflicting with the requirement of higher modulating voltage, it is likely that there is not much improved to be had by either gain nor amplitude. That leaves the CNR at the photodetector. As this means higher laser power, safety aspects might be hindering.

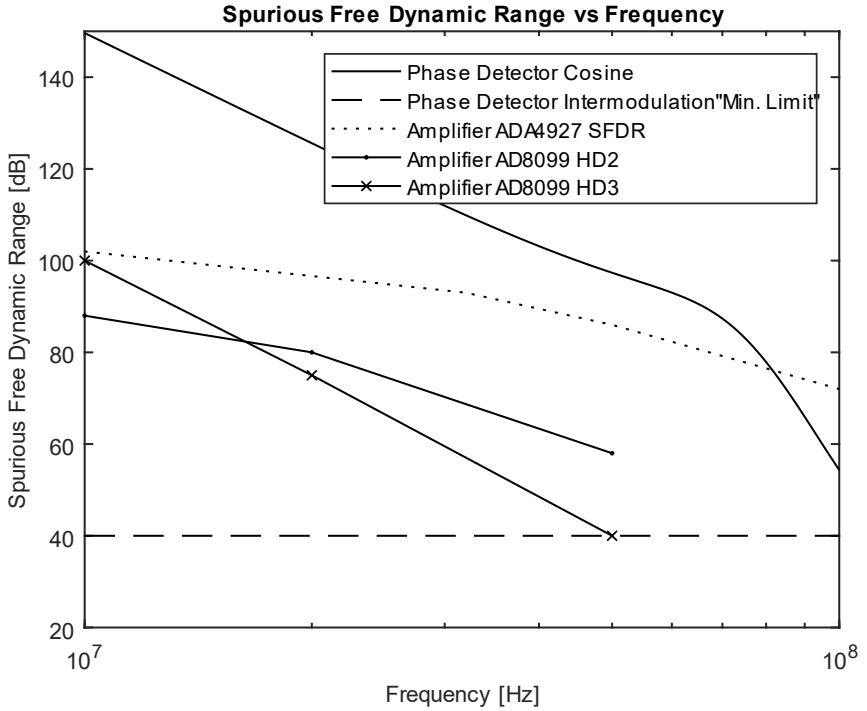

Figure 37 –Spurious free dynamic range for different sources in the high frequency signal chain.

The last figure of merit to consider is the spurious free dynamic range. It is, however, difficult to determine as neither the intermodulation products from the mixer, nor the distortion caused by a non-flat transfer function through the optical chain, are properly analyzed. The distortion sources which are analyzed can be seen in Figure 37. The amplifier's rating are taken from their datasheet, "Phase Detector Intermodulation" refers to the limit given by Equation 40 and "Phase Detector Cosine" is the SFDR due to the phase detector's cosine relationship described by Equation 37.

The phase detector input power is set to produce a minimum SFDR of 40 dB. It remains to be seen how accurate the estimation is, but the intermodulation products are expected to be the limiting factor in the entire signal chain. Since the loop gain is high, the spurs from the phase detection itself, described by Equation 37, is seen to be small except at the end of the passband. As for the amplifiers, the differential amplifier AD4927 is seen to have excellent SFDR. SFDR is not given in the datasheet for the single ended amplifier, AD8099. It does, however, list second and third order distortion. If one assumes an ideal relationship between HD2 and IM3, the amplitude of the IM3 products would be a few dB below the HM2 products. Thus, the HM2 rating may then be used to approximate the SFDR for the AD8099.

5.5 The Prototype

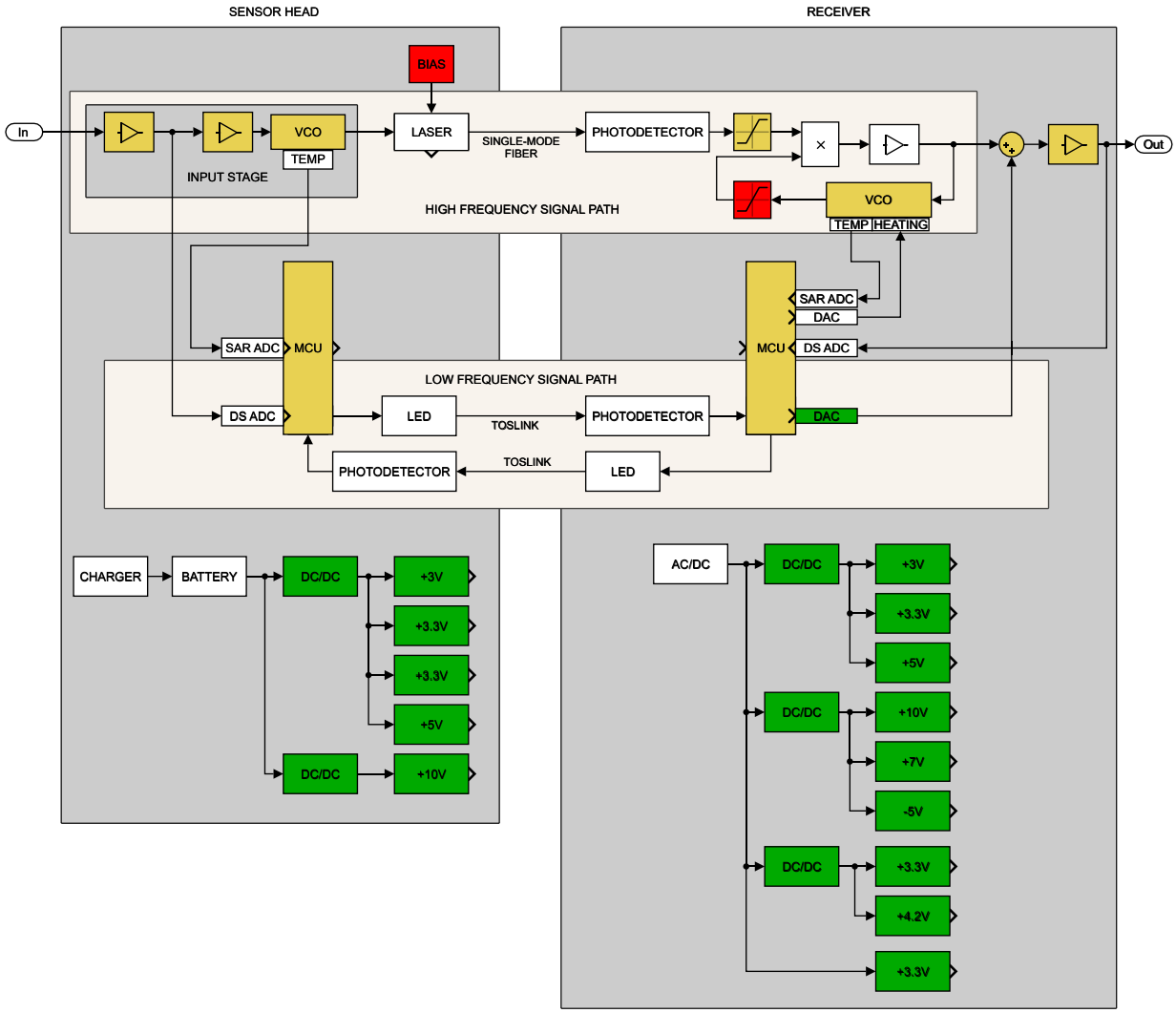

Figure 38 – Block view of the prototype showing which parts have been debugged.

A prototype is constructed but has not been debugged to a degree that permits meaningful measurement results. Several aspects of the prototype do, however, work as expected and these include power rails, processors, output stage and receiver DAC. The main factor limiting a full scale test of the prototype, besides time aspects, is the high frequency path. The laser bias current controller needs a current mirror on its output as the laser anode is (internally) tied to the incorrect polarity. Furthermore, the limiting amplifier inside the PLL loop does not work as expected and thus hinders a separate test of the PLL.

The status of the prototype is schematically shown in Figure 38. Green corresponds to a block which has been debugged thoroughly, red, a fault, yellow, a partially tested block and, white, a block which has not been tested at all.

Chapter 6
Conclusions

The thesis purpose is only partially fulfilled. A measurement probe is indeed designed, and a solid basis for design choices is presented, but the prototype is not fully functional. It is believed that the design is fundamentally sound, but failure to appreciate the time requirements involved has led to insufficient time to properly debug it.

In hindsight, it is also dubious that FM is a suitable transmission method. While the proposed system can offer 11-bit resolution, if larger input levels are allowed, it has limited bandwidth. The limit is imposed mainly by the CNR of the RF signal, leaving 100 MHz as an approximate upper limit. Increasing the CNR may be possible but would require a custom fiber-optic link. Furthermore, the complexity of the full system is also hindering in terms of reliability and development time.

An interesting alternative would be a fully digital system. ADC's and DAC's employing JESD protocols can sustain data rates in the GHz range. Since the protocol has embedded clock, fiber optic ethernet modules, such as SFP, can be used with minimum glue logic. To comply with the high power demand, power over fiber devices can be used. Their considerable cost will, however, limit the range of applications. Even so, it would constitute a considerably more robust, and of higher performance, solution than what is presented in this thesis.

It is also worth mentioning that if high speed is not necessary, a TOSLINK fiber optic link together with a low speed ADC will offer a very easily implemented, and cost-effective, solution. Given low enough speed, it may also be possible to power the sensor head by regular signal photodiodes.

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